On The Study of a Digitally Calibrated R-2R Ladder Architecture

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***Abstract*—This paper presents a study on a digitally calibrated DAC, based on a strictly R-2R topology that is able to derive high resolution – high performance DACs, in terms of INL and DNL. It has been proven by simulations that the performance of the conventional R-2R DAC can be optimized, regardless of resistors' tolerance and the DAC resolution.**

I. Introduction

A Digital to Analog Converter (DAC) is a significant building block that can be found almost in every modern system playing significant role to its overall performance. The quality of the DAC basically depends on the tolerance of the technology used for its implementation and is characterized by the Integral Non-Linearity (INL) and Differential Non-Linearity (DNL) errors as well as by other, second order parameters, such as the Spurious Free Dynamic Range (SFDR), the Signal-to-Noise Ration (SNR) and the conversion time.

High performance, in terms of linearity and high resolution, DACs are implemented using $\Delta\Sigma$ techniques [1], [2] or dynamically calibrated current sources [3], at the cost of slow conversion speed.

High conversion speed can be achieved by using either thermometer code [4]-[6] or ladder DACs [7], [8]. The first architecture has much better linearity at the expense of area and power dissipation, while the second one is characterized by convenient design, low cost and area efficiency.

The combination of the above two architectures derives a hybrid DAC [9], [10] that compromises the linearity and the area tradeoffs regarding with the resolution.

However, high resolution linear DACs can not be achieved by using the above techniques, unless expensive manufactory procedures are employed (laser trimming) [11].

This paper proposes an extension of the conventional R-2R architecture, invoking branches for digital calibration, able to be implemented using all MOS ladders as it is proposed by [12]. The resulted architecture is a strictly based on the R-2R, area efficient, topology that, theoretically, is able to implement high performance, high resolution DACs, in terms of INL and DNL. Additionally, simulations of the proposed architecture and empirical formulas that enable us to forecast the performance of the DAC as a function of the technology tolerance and resolution, are presented.

II. Properties Of The Conventional R-2R Ladder

A study and simulation results of the R-2R ladder are presented in this paragraph and its performance as a function of resistors' tolerance and the resolution is derived, assuming that there is no resistance difference at the switches.

A conventional N-bits R-2R Ladder is depicted in Fig. 1.

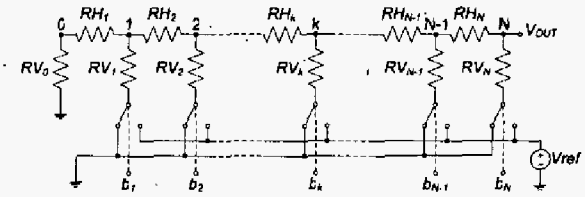

Fig. 1. A conventional N-bits Ladder topology.

We denote RL_k the resistance at the left of the node-k as:

$$RL_k = \begin{cases} RV_0, & k = 0 \\ RV_k // (RH_k + RL_{k-1}), & k = 1,2,\ldots,N. \end{cases} \quad (1)$$

Assuming that only the k-bit is active, the ladder's output voltage will be given as follows:

$$V_{OUT}(k) = Vref \cdot Q_k, \quad (2)$$

where:

$$Q_k = \frac{RH_k + RL_{k-1}}{RV_k + (RH_k + RL_{k-1})} \times \prod_{m=k+1}^{N} \frac{RV_m}{RV_m + (RH_m + RL_{m-1})}. \quad (3)$$

Subsequently the output voltage of the ladder, for each possible digital input word(D), due to the contribution of all the bits $(b_1, b_2, \ldots, b_N)$, equals to:

$$V_{OUT}(D) = \sum_{k=1}^{N} b_k V_{OUT}(k),\ D = \sum_{k=1}^{N} b_k 2^{k-1}. \quad (4)$$

Thus, the Thevenin equivalent of a ladder is an ideal voltage source $V_{OUT}(D)$ in series with a resistor $RL_N \cong R$.

Taking into consideration (4) we can calculate the INL using:

$$\mathrm{INL} = \max\left|\frac{V_{OUT}(D) - V_{OUT}(0)}{Vref} - \frac{D}{2^N}\right|, \quad (5)$$

expressed in LSBits, where $0 < D < 2^N - 1$, while the DNL is given by:

$$\mathrm{DNL} = \max\left|\frac{V_{OUT}(D+1) - V_{OUT}(D)}{Vref}2^{N-1} - 1\right|, \quad (6)$$

expressed in LSBits as well, where $0 < D < 2^N - 2$.

Applying the above formulas we simulated the ladder performance for a range of tolerances and resolutions. After statistical processing on the simulated results, the behavior of the INL's mean value and deviation, as a function of resistors' tolerance T and resolution N was derived and are shown in Fig. 2 and 3.

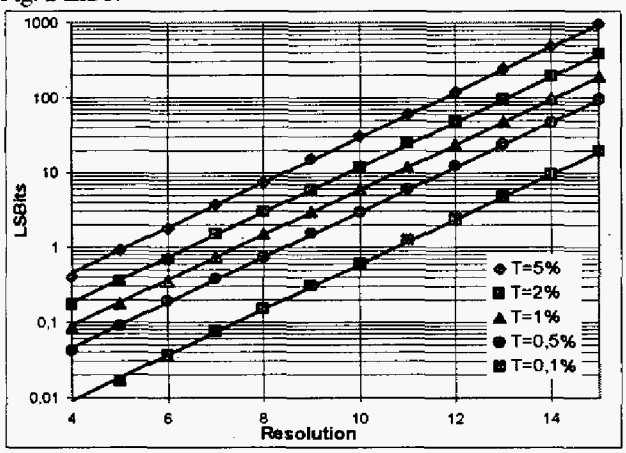

Fig. 2. Mean INL value as a function of resolution for several resistor's tolerances.

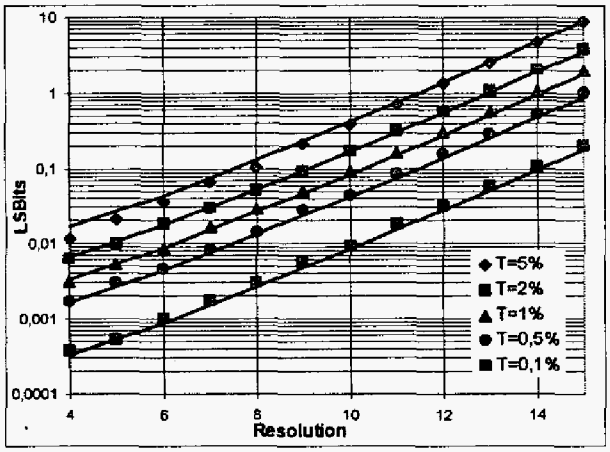

Fig. 3. Deviation of INL as a function of resolution for several resistor's tolerances.

Additionally, we found out that the empirical formulas (7) and (8) fit on the statistical results for the INL mean value and deviation:

$$\overline{\mathrm{INL}}(T,N) = 0{,}577 \cdot T \cdot 2^N \qquad (\mathrm{LSBits}), \quad (7)$$

$$\sigma_{\mathrm{INL}}(T,N) = 0{,}082 \cdot T \cdot \frac{2^N}{N} \qquad (\mathrm{LSBits}). \quad (8)$$

Markers in Fig. 2 depict the INL simulated mean value, while lines depict the graph of (7). Similarly, markers and lines in Fig. 3 depict the INL's deviation according to simulation results and (8), respectively. It can be seen that empirical formulas fit well on the simulated results.

Simulations regarding the DNL exhibited identical statistical results and subsequently, resulted in identical empirical formulas. Equations (9) and (10) are the corresponding formulas for the DNL's mean value and deviation, respectively.

$$\overline{\mathrm{DNL}}(T,N) = 0{,}639 \cdot T \cdot 2^N \qquad (\mathrm{LSBits}), \quad (9)$$

$$\sigma_{\mathrm{DNL}}(T,N) = 0{,}101 \cdot T \cdot \frac{2^N}{N} \qquad (\mathrm{LSBits}). \quad (10)$$

The above empirical formulas could be used to estimate the performance of a ladder, taking into account resistors' mismatch and resolution.

III. Architecture Of The Digitally Calibrated DAC

Fig. 4 depicts an NR-bits DAC of the proposed architecture. It can be seen that an NR-bits ladder identical to this in Fig. 1 is employed, where k $(k = 1,2,\ldots,NR)$ vertical resistor RV_k has been substituted by an R-valued R_AV_k resistor in series with an NC-bits ladder, named as k-calibration ladder, of an also R-valued output resistance, R_BV_k.

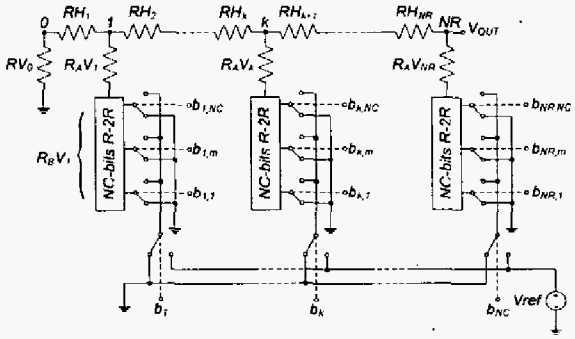

Fig. 4. Architecture of the proposed digitally calibrated Ladder.

In more details, R_AV_k is half the RV_k of the conventional ladder, while R_BV_k represents the output resistance of the k-calibration ladder, which is theoretically equal to R, as it has been proved in (1). Thus, the functional behavior of the proposed calibrated ladder remains the same with the conventional one, as depicted in Fig. 5.

This topology provides the advantage of trimming the reference voltage VC_k for each resolution bit k, by assigning a different digital word (Digital Calibration word – DC_k), to the corresponding calibration ladder. Consequently, the contribution of each resolution bit at the output voltage can be adjusted so as to cancel resistors mismatch; meaning that an

accurate adjustment of the reference voltage is able even to eliminate the non-linearity behavior.

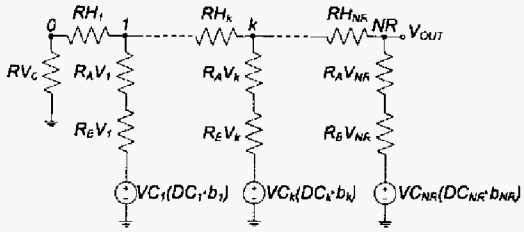

Fig. 5. Thevenin equivalent of the proposed architecture.

Since the reference voltage of each bit can be trimmed with a resolution of NC -bits, the length of each calibration ladder should apparently be selected so as to derive the desired linearity.

IV. Calibration Principles

The goal of a calibration procedure, regarding the proposed architecture, is the estimation of the DC_k calibration word that forces k -calibration branch to contribute a voltage at the output of the ladder, as close as possible to the ideal. Assuming that $Vmax$ is the maximum output voltage of the DAC, the contribution $V_{OUT}(k)$ of the k -branch, applying (2), should be as close as possible to the value assigned by (11),

$$V_{OUT}(k) = VC_k(DC_k) \cdot Q_k = 2^{k-NR-1} \cdot Vmax. \quad (11)$$

In other words the normalized voltage contribution $V_{NORM}(k)$ of each bit should ideally be the same,

$$V_{NORM}(k) = 2^{NR+1-k} \cdot V_{OUT}(k) = Vmax. \quad (12)$$

Since the MSBit plays the most significant role to the DAC performance, the selection of $Vmax$ should exactly fit to a normalized voltage that MSBit is able to derive applying the calibration word DC_{NR}.

$$Vmax = 2 \cdot V_{OUT}(NR) = V_{NORM}(NR) \quad (13)$$

Moreover, the normalized voltage contributions of the rest bits should closely approximate $Vmax$. Thus, $Vmax$ should be less or equal to the minimum normalized voltage contribution regarding all the resolution bits,

$$Vmax \le \min_{k=1,\dots,NC} \{V_{NORM}(k)\}. \quad (14)$$

$Vmax$ derived by (13) and (14) is the reference voltage of the calibrated ladder in terms of the conventional ladder, since this will be the maximum voltage at the output of the calibrated ladder. DC_{NR} is the calibration word for the calibration branch at the MSBit of the ladder. The calibration words for the least significant calibration branches should be selected so as to comply with

$$VCn_k(DC_k) \cong VC_{NR}(DC_{NR}). \quad (15)$$

Following the above guidelines we simulated the DAC performance of the proposed architecture for various resolutions and for various resolutions of the calibration branches.

V. Statistical Processing Of The Simulation Results

Several simulations, using formulas described in II and calibration guidelines issued in IV, were applied on this DAC architecture for a range of tolerances, DAC resolutions and calibration resolutions. All simulations were issued using the same length for all the calibration branches. The statistical processing of the simulation results indicates that increasing the resolution of the calibration branches, the linearity of the DAC, in terms of INL and DNL, follows an exponential improvement. Similarly to Fig. 2, Fig. 6 depicts the simulated mean INL value for a tolerance $T = 0.01$ (1%) and for various resolutions of the calibration branches.

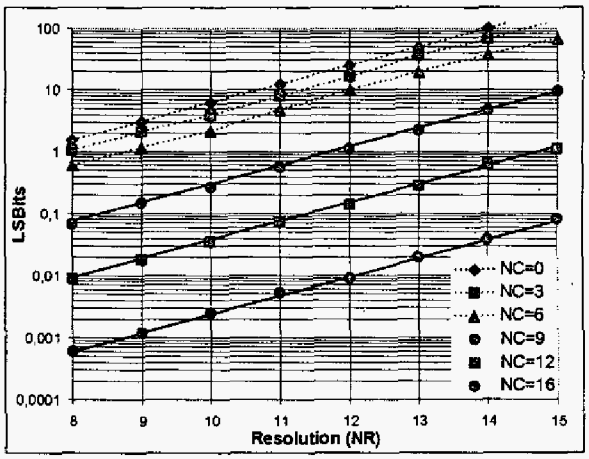

Fig. 6. Mean INL value as a function of DAC resolution (NR) for several calibration resolutions and resistor's tolerance equal to 1%.

Fig. 7 depicts the mean value of INL as a function of the resolution NC of the calibration branches for a tolerance $T = 0.01$ (1%). Apparently, the exponential improvement of the INL is observed for a calibration resolution above 5-bits, whereas below 5-bits the improvement becomes negligible, thus resulting to the break-points depicted in this figure. The cause that generates these break-points is that the calibration algorithm is unable to trim the reference voltages, when the calibration resolution is not adequate, regarding the resistor tolerance. Thus, all the calibration words are forced to be $2^{NC} - 1$.

Simulations proved that the position of a break-point, thus the minimum length required for the calibration ladders in order to be able to improve the DAC linearity, depends on the tolerance of the resistors employed. Empirical inequality (16) defines the minimum number of bits NC, required for the calibration ladders, as a function of the tolerance T.

$$NC \ge -1.68 - \log_2 T \quad (LSBits) \quad (16)$$

Evaluating (16) using $T = 0.01$, as is considered in Fig. 7, we derive that NC should be greater than 4.96 bits.

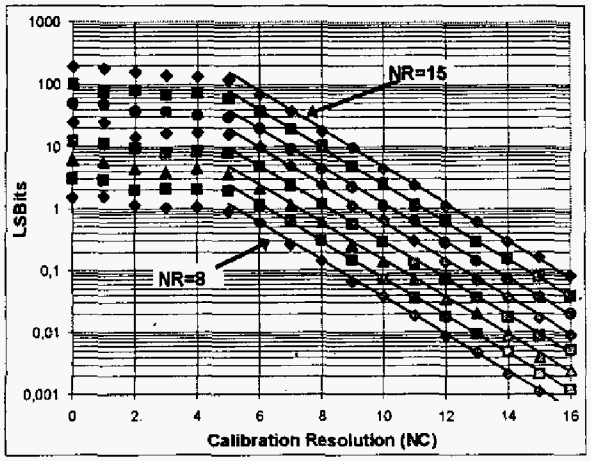

Fig. 7. Mean INL value as a function of calibration resolution for several DAC resolutions (NR)and resistor's tolerance equal to 1%.

The empirical formulas (17) and (18) fit on the statistical results for the INL and DNL mean values, assuming that NC complies with inequality (16).

$$\overline{\mathrm{INL}}(NR,NC,T) = 1.476 \cdot T \cdot 2^{NR-NC} \text{ (LSBits)} \quad (17)$$

$$\overline{\mathrm{DNL}}(NR,NC,T) = 1.566 \cdot T \cdot 2^{NR-NC} \text{ (LSBits)} \quad (18)$$

Thick lines in Fig. 6 and 7 are the plot of (17), while markers represent the statistical values derived by the simulations.

Finally, we can conclude that the linearity of the proposed architecture could also be derived by (7) and (9), on the condition that tolerance T equals to an equivalent tolerance T_e

$$T_e = 2.56 \cdot T \cdot 2^{-NC}. \quad (19)$$

VI. Further Considerations

The proposed architecture demands a significantly reduced area for its implementation, since the total number of components required, is proportional to the square of the resolution length, while the number of components required by a thermometer code DAC is exponentially proportional to its resolution.

The use of the same resolution for all the calibration branches is not obligatory. It has been found by simulations that the least significant bits are not so sensitive to the selection of the calibration word. Thus, less resolution for the LS-branches may be employed without affecting the overall performance. This will also lead to an additional reduction of the component count.

The presented architecture concerns voltage mode DACs; however it can also be applied, as it is, to current mode DACs of similar architecture.

Moreover, the adopted calibration procedure could be further extended in order to provide even better performance. A weighted least square algorithm could be employed for selecting the appropriate calibration words, thus deriving the best matching of the normalized voltages $V_{OUT}(k)$.

Finally, it is of great interest to study the behavior of the proposed DAC when taking into account the switch resistor difference. It is expected that this difference will degrade the performance of the proposed DAC. However, it will still be able to come up with much better INL and DNL characteristics in contrast with those of the conventional one.

VII. Conclusion

In this paper we presented an area efficient DAC architecture strictly based on the R-2R ladder topology attaining at the same time high performance, high resolution and low cost. Additionally, empirical formulas were derived for estimating the conventional and the digitally calibrated ladders' performance as a function of the technology's tolerance and the desired resolution. Implementation of the presented architecture in a chip and measurements to qualify the real performance of the DAC, in terms of accuracy and speed, is of further work.

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References

[1] I. Fujimori and Tetsuro Sugimoto, "A 1.5 V, 4.1 mW dual-channel audio delta-sigma D/A converter," IEEE J. Solid State Circuits, vol. 33, Dec. 1998.

[2] T. Shui, R. Schreier and F. Hudson, "Mismatch shaping for a current-mode multibit delta-sigma DAC," IEEE J. Solid State Circuits, vol. 34, Mar. 1999.

[3] M. P. Tiilikainen, "A 14-bit 1.8-V 20-mW 1-mm² CMOS DAC," IEEE J. Solid State Circuits, vol. 36, Jul. 2001.

[4] C. Lin and K. Bult "A 10-b, 500-msample/s CMOS DAC in 0.6 mm²," IEEE J. Solid State Circuits, vol. 33, Dec. 1998.

[5] A. Bosch, M. Borremans, M. Steyaert and W. Sansen, "A 10-bit 1-Gsample/s Nyquist current-steering CMOS D/A converter," IEEE J. Solid State Circuits, vol. 36, Mar. 2001.

[6] J. Bastos, A. M. Marques, M. Steyaert and W. Sansen, "A 12-bit intrinsic accuracy high-speed CMOS DAC," IEEE J. Solid State Circuits, vol. 33, Dec. 1998.

[7] L. Wang, Y. Fukatsu and K. Watanabe, "Characterization of current-mode CMOS R-2R ladder digital-to-analog converters," IEEE Trans. Instr. and Meas., vol. 50, Dec. 2001.

[8] M. P. Kennedy, "On the robustness of R-2R ladder DAC's," IEEE Trans. Circuits & Syst. II, vol. 47, Feb. 2000.

[9] Y. Cong and R. L. Geiger, "A 1.5 V 14-bit 100ms/s self-calibrated DAC," IEEE J. Solid State Circuits, vol. 38, Dec. 2003.

[10] A. R. Bugeja and B. Song, "A self-trimming 14-b 100-MS/s CMOS DAC," IEEE J. Solid State Circuits, vol. 35, Dec. 2000.

[11] "R/2R ladder networks," Application Note AFD006, International Resistive Company, Inc., 1998.

[12] K. Bult and J. Geelen, "An inherently linear and compact MOST-only current division technique," IEEE J. Solid State Circuits, vol. 27, Dec. 1992.