A Digitally Calibrated R-2R Ladder Architecture for High Performance Digital-to-Analog Converters

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***Abstract*—The paper presents a new model for R-2R ladder-based digital-to-analog converters, developed in terms of resistors' tolerance. The widely used R-2R ladders are easy to be realized as an integrated circuit, while their performance is basically limited due to the resistors' mismatch. However, it is possible to achieve higher linearity, in terms of Integral and Differential Non-Linearity errors, if calibration is employed. In this paper, the conventional R-2R ladder architecture is briefly discussed, and then a new digitally calibrated architecture is presented with its calibration algorithm, based on the resistors' tolerance formulation. It has been proven by simulations that the performance of an R-2R-based digital-to-analog converter can be optimized regardless of the resistors' tolerance and the required resolution.**

I. INTRODUCTION

The performance of a digital-to-analog converter (DAC) plays significant role to almost every modern system design. One of the most popular methods for converting a digital word into a quantized analog signal is based on R-2R ladder networks. These ladders have the significant advantage of being easily integrated onto a small silicon area, as they require a small device count, and therefore constitute key components in mixed analog and digital ASICs.

Nowadays digital-to-analog conversion demands high performance in terms of linearity, resolution and speed conversion, which are not easy to be straightforwardly implemented. Although R-2R ladder-based DACs and especially current-output ladders can inherently operate as high-speed current dividers [1], they are not able to meet the linearity and resolution requirements.

ΔΣ techniques [2] or dynamically calibrated current sources [3] are mainly employed to provide high performance, in terms of linearity and high resolution, but at the cost of slow conversion speed. On the other hand, high conversion speed with high performance can be achieved using either thermometer code DACs [4], at the expense of area and power dissipation, or laser-trimmed R-2R ladder-based DACs, using expensive manufactory procedures [5]. Another compensating method includes hybrid DACs [6] or self-calibrated R-2R ladders [7].

The motivation of the work is to increase the linearity, in terms of Integral/Differential Non-Linearity (INL/DNL) errors and resolution of the conventional R-2R ladder, concluding in a high performance, easily integrated DAC architecture. The proposed architecture extends the conventional ladder with R-2R branches for digital calibration and concludes in a strictly R-2R-based, area efficient topology, able to implement high performance, high resolution DACs.

II. PRELIMINARIES

Fig. 1 shows the conventional R-2R ladder DAC. V_{ref} is the reference voltage and b_k (k=1…N) is the N-bit digital word to be converted into the analog voltage.

Assuming that all resistors are perfectly matched and the switches are ideal, the output of the ladder will be

$$V_{out} = \left(b_1 2^{-N} + \ldots + b_N 2^{-1}\right) V_{ref} = V_{ref} \sum_{k=1}^{N} b_k 2^{k-N-1}, \quad (1)$$

since the impedance seen from the k-node to the left is 2R and the reference voltage switched by b_k is attenuated by 2^{-k} to reach the output. The contribution of the k-bit to the output voltage is

$$V_{out}(k) = V_{ref} Q_k, \; k = 1..N, \quad (2)$$

where

$$Q_k = \frac{RH_k + RL_{k-1}}{RV_k + (RH_k + RL_{k-1})} \prod_{m=k+1}^{N} \frac{RV_m}{RV_m + (RH_m + RL_{m-1})} \quad (3)$$

and

$$RL_k = \begin{cases} RV_0, & k=0 \\ RV_k // (RH_k + RL_{k-1}), & k=1\ldots N. \end{cases} \quad (4)$$

Now the output of the ladder will be given by

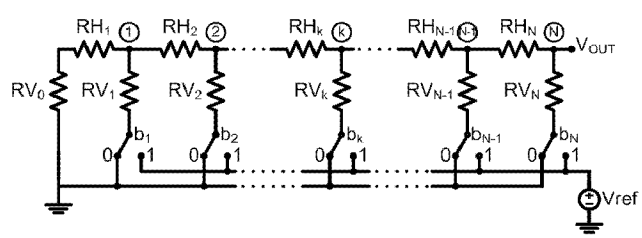

Figure 1. Conventional R-2R ladder DAC.

$$V_{out}=\sum_{k=1}^{N} V_{out}(k)=\sum_{k=1}^{N} Q_k V_{ref} . \quad (5)$$

Simulations for a range of resistors' tolerance (T) and resolutions (N), followed by statistical analysis based on the above formulation of an R-2R ladder network, proved that the INL's and DNL's mean value can be approximated by

$$\overline{INL}(T,N)=0.577\,T\,2^N\,(LSBits) \quad (6)$$

$$\overline{DNL}(T,N)=0.639\,T\,2^N\,(LSBits), \quad (7)$$

while their deviation has been expressed by similar formulas. These empirical formulas enable the forecast of a ladder's linearity given the resistors' tolerance and resolution.

III. Architecture Of The Digitally Calibrated R-2R Ladder

Equation (5) points out that the trimming of the reference voltage for each bit is able to equalize the error of the Q_k factors, introduced by the resistors' mismatch, in such a way that the voltage contribution of each bit to the output voltage is as close as possible to the optimum value.

Based on the above ascertainment, the proposed architecture has been designed so as to enable the trimming of the reference voltage for each resolution bit. Fig. 2 depicts an NR-bits ladder of the proposed architecture. A conventional NR-bits ladder is employed, where each of the NR-vertical resistors RV_k (k=1…NR) has been replaced by an in series combination of an R-valued resistor R_AV_k and an NC-bits ladder, named as k-calibration ladder.

R_AV_k is R-valued, while R_BV_k represents the output resistance of the k-calibration ladder, which is also R-valued (4). Thus, the proposed architecture retains the functional principle of the voltage/current division from the k-node to the left.

The Thevenin equivalent of the proposed architecture, shown in Fig. 3, indicates that the reference voltage VC_k, for each resolution bit k, can be trimmed by assigning a different Digital Calibration word (DC_k) to the corresponding calibration ladder. The proper selection of each DC_k-word is

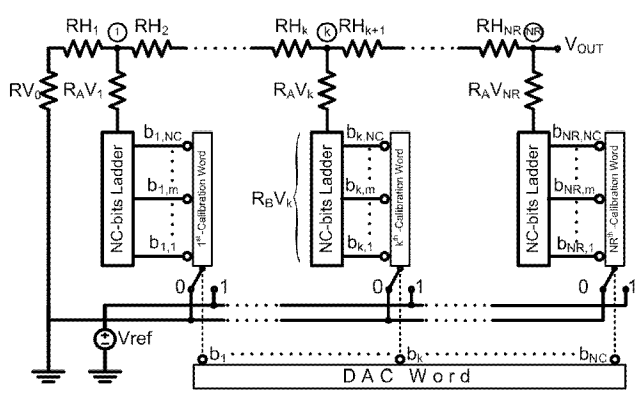

Figure 2. Architecture of the proposed digitally calibrated ladder.

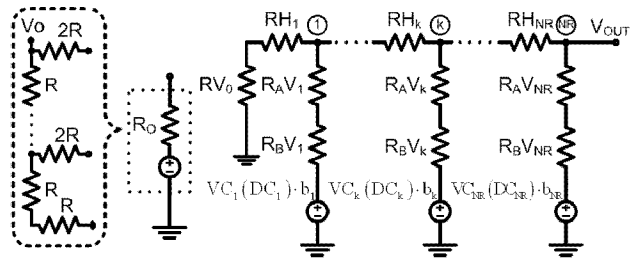

Figure 3. Thevenin equivalent of the proposed architecture.

able to adjust the contribution of the corresponding resolution bit at the output voltage of the ladder; so as to cancel non-linearity effects of resistors' mismatch. Thus, a one-time accurate adjustment of the reference voltage, for each resolution bit, can eliminate permanently the inherently non-linear behavior of the R-2R ladder.

Since the reference voltage of each resolution bit can be trimmed at 2^{NC} different voltage values, the selection of the length NC for each calibration ladder is a major issue that can be encountered by the designer. Many policies could be applied; stepwise, linear or even logarithmic lowering of the calibration length for the low order resolution bits are possible solutions for even more area effective designs. The calibration technique, described in the next section, is independent of the length of each calibration branch. However, all simulations were performed assuming identical NC for all the calibration branches.

IV. Calibration

The goal of a calibration procedure, taking into account the proposed architecture, is the estimation of the DC_k calibration word that forces k-calibration ladder to contribute a voltage at the output, as close as possible to the ideal. Assuming that $V_{Full\ Scale}$ is the maximum output voltage of the ladder and applying (2), the contribution $V_{OUT}(k)$ of the k-branch (k=1…NR) should be as close as possible to the value

$$V_{OUT}(k)=VC_k(DC_k)Q_k \approx 2^{k-NR-1}V_{Full\ Scale} . \quad (8)$$

Obviously, the normalized voltage contribution $V_{NORM}(k)$ for all resolutions bits should ideally have the same value

$$V_{NORM}(k)=2^{NR+1-k}V_{OUT}(k) \approx V_{Full\ Scale} . \quad (9)$$

Since the MSBit plays the most significant role to the ladder linearity, the selection of $V_{Full\ Scale}$ should fit exactly to a normalized voltage that MSBit is able to produce, applying the calibration word DC_{NR}.

$$V_{Full\ Scale} \equiv 2V_{OUT}(NR) \equiv V_{NORM}(NR) . \quad (10)$$

Additionally, the normalized reference voltages that the rest of the resolution bits (except for the MSBit) can produce should closely approximate $V_{Full\ Scale}$. Thus, the possible $V_{Full\ Scale}$ from (10) should also be less or equal to the minimum normalized reference voltage, taking into account all the resolution bits, apart from the MSBit (k=1…NR-1),

$$V_{\text{Full Scale}} \le \min\left\{2^{NR+1-k} VC_k \left(2^{NC}-1\right)\right\}. \qquad (11)$$

$V_{\text{Full Scale}}$, derived by (10) and (11), is the reference voltage of the calibrated ladder in terms of a conventional ladder, since this will be the maximum voltage at its output. $V_{\text{Full Scale}}$ will not be equal to Vcc; yet this is not a great disadvantage, as DAC design emphasizes more on its linearity rather than on its output gain, which can be externally adjusted.

Taking into account the resulted $V_{\text{Full Scale}}$ and applying k=NR in (8), the calibration word for the most significant calibration ladder (DC_{NR}) is determined, while all the other calibration words (k=1…NR-1) should be selected using the criterion

$$\left|2^{NR-k} VC_k \left(DC_k\right) Q_k - V_{OUT}\left(NR\right)\right| \to 0. \qquad (12)$$

The above criterion constitutes the basic requirement for the discussed calibration algorithm, as the trimming of the reference voltages, managed by the calibration ladders, targets at the accomplishment of the above criterion, so as the remained error from the NR-1 voltage differences results in extensively decreased non-linearity effects.

V. Error Considerations Of The Calibration Algorithm

The presented calibration algorithm takes into account only the resistors' tolerance. Thus, the analysis is limited to the basis of the resistors' tolerance and resolution as well. Apparently, the formulation of a ladder is a more difficult task, when more error sources are involved. An exhaustive, but complete, analysis of the ladder network should also take into consideration the non-linear behavior of the switches and the R_{ON} effect of a MOST-only implementation as well.

Nevertheless, the adopted calibration procedure could be further extended, if weighted least square root algorithm would be employed for selecting the proper calibration words, thus deriving a further more better matching of the normalized voltage outputs than (12) dictates.

Finally, in practice, a measurement device should be utilized in order to determine the best resolution bit voltage contribution at the output of the ladder. Since every measurement device has finite accuracy, another error source is added. However, simulation results, presented in the next section, prove that the proposed architecture is able to come up with improved characteristics, in terms of INL, DNL and resolution, over against the conventional ladder.

VI. Simulation Results

Several simulations for the digitally calibrated ladder architecture were performed using formulas described in II and the calibration algorithm discussed in IV, for a range of resistors' tolerance (T=0.1%, 0.2%, …,2.0%), resolutions (NR=8, 9, …, 15) and calibration lengths (NC=1, 2, …, 16).

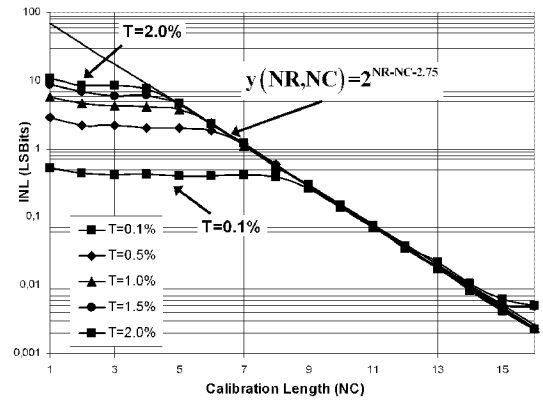

Figure 4. Simulated mean INL value for 10-bits resolution at various resistors' tolerance.

The above simulations were transacted assuming the same length for all the calibration ladders.

Fig. 4 depicts the simulated mean INL value as a function of the calibration length (NC) for various resistors' tolerance (T), assuming 10-bits resolution (NR). A particular analysis on the simulation results implies that the proposed ladder's behavior is twofold:

- Calibration ladders are not inherently able to offer a satisfying reference voltage trimming, when their length is not adequate. Thus, the employed calibration algorithm forces all calibration words to the certain value of 2^{NC}-1 and consequently ladder's linearity is only affected by the resistors' tolerance; which is the case of the conventional ladder. Any negligible improvement may take place only because of the more complex resistor network that the proposed architecture utilizes.
- When the calibration length is adequate, calibration ladders achieve an exponentially improved linearity due to the reference voltage trimming. It is remarkable that, in this case, ladder's linearity depends only on the calibration length, independently of the resistors' tolerance; at least in the range of the performed simulations. Diagonal line ($2^{NR-NC-2.75}$) in Fig. 4 fits on the INL exponential improvement due to the corresponding calibration length.

This remarkable fact can be intuitively explained taking

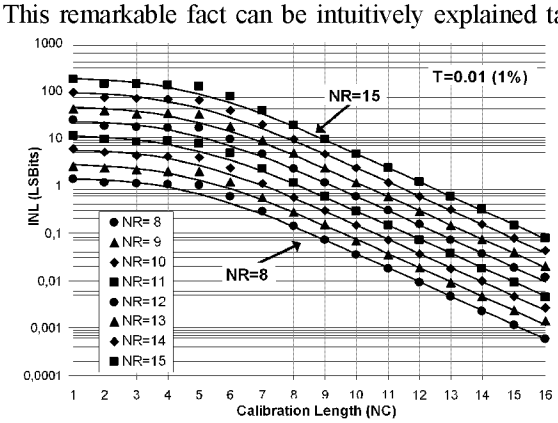

Figure 5. Simulated INL mean value for resistors' tolerance T=0.01 (1%) for various resolutions.

into consideration that the linear increment of the length for each calibration ladder constitutes an exponentially increased possibility to accomplish the criterion asserted by (12). This results in an exponentially improved linearity of the proposed ladder, since an exponentially improved matching between the normalized voltages of each resolution bit and the MSBit occurs.

Further statistical analysis of the above simulation results indicates that the predictable exponential improvement in ladder's linearity is forced when the length of the calibration ladders complies with

$$NC \geq 7.887\text{-}NR\text{-}\log_2(T), \tag{13}$$

while the behavior of the proposed ladder, regarding the INL and DNL mean value, can be compactly approximated by

$$INL(NR,T,NC) = \frac{0.577\,T\,2^{NR}}{1+0.577\,T\,2^{NC+2.75}}, \tag{14}$$

$$DNL(NR,T,NC) = \frac{0.639\,T\,2^{NR}}{1+0.639\,T\,2^{NC+2.75}}. \tag{15}$$

Lines in Fig. 5 represent the plot of (14) for various resolutions NR, while markers stand for the corresponding simulated mean INL value. Apparently, (14) is able to predict with high precision the linearity of the digitally calibrated ladder. However, it should be emphasized that (14) and (15) comply with the results within the range of the performed simulations. It is of further work to confirm or modify these empirical formulas for a wider range of resistors' tolerance and calibration lengths.

VII. Characterization Of The Digitally Calibrated Ladder

An area comparison, in relation with common ladder topologies, via the required component count, can be performed as depicted in Fig. 6. The proposed architecture requires a quite suppressed total component count in relation with the popular R-String DAC for implementing high resolution DACs, while at the same time an improved overall performance is attained.

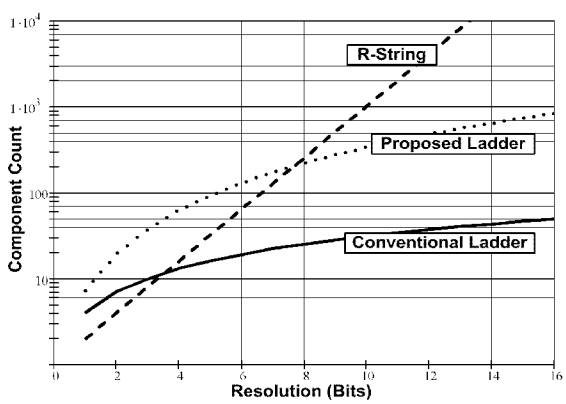

Figure 6. Component count comparison for 3 DAC topologies.

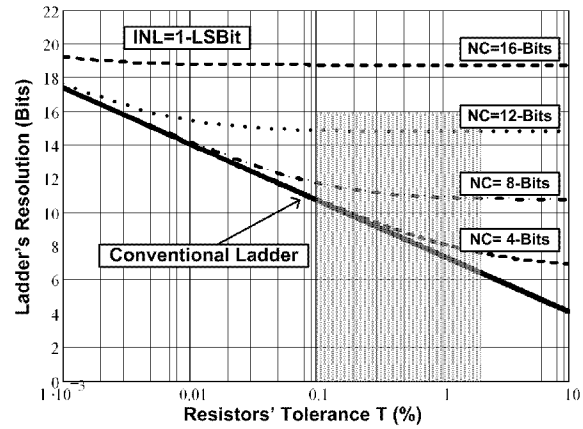

Figure 7. Conventional and the proposed ladder's performance.

Additionally, the performance of the proposed and the conventional ladder can be straightly correlated with the resolution capabilities, on demand of the crucial value of 1-LSBit INL, as depicted in Fig. 7. Thick line in Fig. 7 depicts the inherent performance limitation of the conventional ladder, while the discontinuous lines present the effect of the calibration technique for various calibration lengths. Shadowed area indicates the simulation range.

VIII. Conclusions

The proposed, strictly based on the R-2R topology, area efficient ladder architecture enables the design of high resolution DACs, attaining at the same time high linearity, regardless of the resistors' tolerance at a quite rational area expense. Empirical formulas were derived for estimating the digitally calibrated ladder's performance, as a function of the desired resolution and the calibration length. Additionally, an algorithm for the required one-time calibration has been presented in details.

Acknowledgment

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