A MOST-Only R-2R Ladder-Based Architecture for High Linearity DACs

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Abstract— **The paper presents a MOST-Only, digitally calibrated DAC architecture, based on the R-2R ladder topology. The proposed DAC architecture employs circuitry that enables the fine trimming of each bit's current contribution at the DAC's output, thus concluding in a high linear DAC architecture. The architecture of the proposed DAC is discussed in details along with simulation results that confirm its high linearity performance. The proposed DAC topology maintains the conventional ladder's performance in speed and power dissipation without requiring large area for its implementation.**

I. INTRODUCTION

Nowadays technology has realized the data processing of almost any system in the digital domain. However, in most cases, systems have to exchange data with the real world thus, data conversion from analog-to-digital and vice versa is mandatory. Significant role to the overall performance of a modern system plays the data converters' characteristics, regarding linearity, resolution, speed and power consumption. Especially digital-to-analog converters (DAC) exist in many systems, however their performance cannot be easily optimized and uniquely determined, since designers have to face trade-offs regarding the performance criteria.

Several digital-to-analog conversion techniques have been presented improving the performance of a DAC. However, none of these techniques is able to satisfy all the requirements. For example, ΔΣ techniques [1] or dynamically calibrated current sources [2] have improved characteristics, in terms of resolution and linearity, while their performance lack of speed. Similarly, ladder DACs [3], [4] can offer high speed operation, small area and low power consumption, but they cannot conform to high resolution and high linearity requirements. On the other hand, high conversion speed along with high linearity can be achieved using either thermometer code DACs [5]-[7], at the expense of area and power dissipation, or laser-trimmed [8] R-2R ladder-based DACs, using expensive manufactory procedures. The most common solution in order to compensate the above requirements is to employ hybrid DACs [9], [10] or self calibrated R-2R ladders [11], thus counterbalancing the strict requirements of the digital-to-analog conversion procedure.

A recently proposed technique [12], which is based on a voltage-mode ladder DAC, improves exponentially its performance, regarding the resolution and linearity, without affecting speed, area and power consumption. Based on this technique, new results regarding a current-mode, MOST only, digitally calibrated R-2R ladder architecture, its design specifications and performance characteristics, are presented in this paper.

This work has been motivated by the increased performance, in terms of speed and linearity, required by several applications. The proposed DAC architecture is meant to be employed with a high performance frequency synthesizer, which is based on the Dual Input Phase Accumulator technique [13]. However, the proposed DAC technique can be employed by any application that requires high linearity, along with high speed and low power, data conversion, assuming any practical resolution.

II. ARCHITECTURE

Fig.1 depicts the current-mode version of the R-2R ladder proposed by [14]. In a conventional design the voltage difference Vref-Vbias is assumed small enough and thus body effect does not affect significantly the mismatching of the FETs' R_{ON}. All FETs are assumed of the same size, while active FETs operate at the linear region.

The architecture proposed by [12] is based on the voltage-mode R-2R ladder, while the current-mode, MOST only version is depicted in Fig.2. In this architecture all FETs related to the R-2R topology are denoted as Q and are of the same size, while they operate at the linear region and have an R_{ON} resistance.

As it can be seen in Fig.2, each switching pair of FETs has been replaced by an NC-bits CMOS current-mode ladder, identical to the one depicted in Fig.1, thus introducing a calibration branch. This replacement does not affect the R-2R topology, since the input resistance of each calibration branch is equivalent with one's FET R_{ON}. The modified topology enables the trimming of the output current of each calibration branch, according to the specific calibration word. Therefore, it is able to trim each branch's current close-enough to the optimum one. Apparently, the resolution of each calibration branch (NC) plays

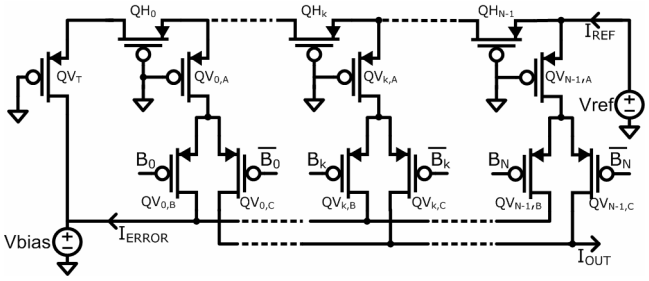

Figure 1. Conventional CMOS-based R-2R ladder DAC.

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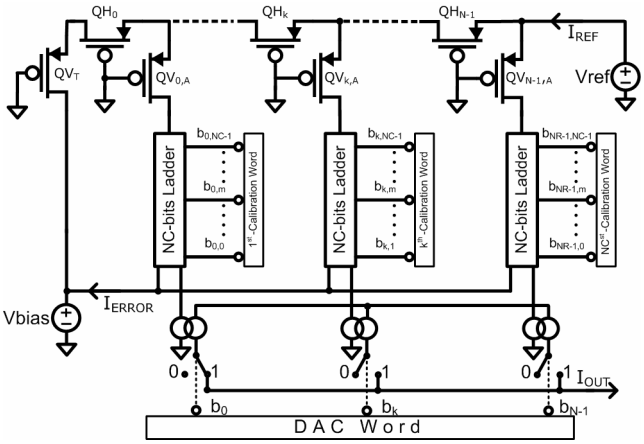

Figure 2. The proposed architecture of the current-mode DAC.

a major role, since it assigns the accuracy of the trimming procedure. Finally, the output currents of each calibration branch are mirrored and summarized at the output of the DAC (I_{OUT}).

Fig.3 indicates that the proposed DAC circuitry consists of a number of identical blocks, one for each DAC bit. Each one of these blocks consists of the corresponding bit's calibration ladder as well as the required circuitry, for current-cascading and the assignment of the calibration word. Digital signals Din, Dout, SCLK and LOAD are responsible for the assignment of the calibration word for each bit. Analog signals Cin and Cout are employed for the current-cascading, while CI_{OUT} is the output current of each block. Finally, the digital signal b_k represents the corresponding bit of the DAC's digital input word.

Each block of Fig.3, depicted in more details in Fig.4, consists of a single element of the DAC backbone (QH_k and $QV_{k,A}$), the calibration branch, composed by NC-similar blocks, one for each calibration bit, and a current mirror (M1 to M6), that mirrors the proper amount of current to the output node, while the error current is let to the ground (through E1 to E3). E1 to E3 and M1 to M6 are of the same size and should be large enough, in comparison with FETs denoted as Q, since they have to operate at the saturation region and preserve the minimum voltage drop across.

Each block, representing a calibration bit in Fig.4, consists of the calibration register and a single bit calibration ladder, as depicted in Fig.5. Calibration register consists of two D-FF's and enables the serial-input/parallel-load of the DAC's calibration words. The single bit calibration ladder is identical to the cell of the ladder depicted in Fig.1.

As soon as the calibration words have been assigned, all FETs, denoted as Q, operate at a steady-state, regardless of the

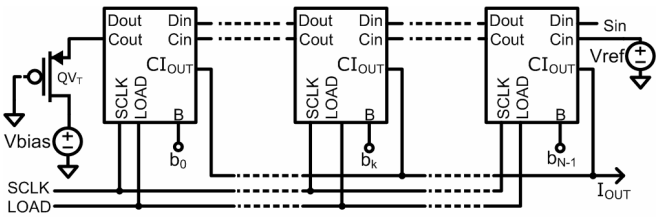

Figure 3. Block diagram of the proposed DAC circuitry.

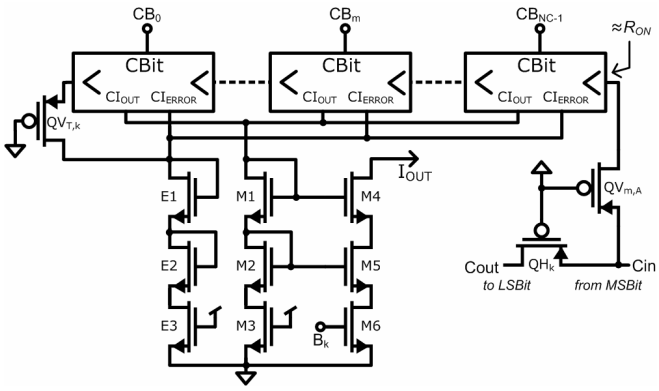

Figure 4. Internal architecture of a ladder's block.

DAC's digital input. Only FETs M4 to M6, of each calibration branch, alternate their operating conditions according to the DAC word. This implies that most of the circuitry operates in constant conditions, as only a small portion of it has to switch; thus contributing to high speed performance. Since current, in most FETs, is constant, the power consumption of the circuit will be approximately equal to $Vref \times I_{REF}$. Depending on the output current of the DAC, extra power consumption, dissipated on FETs M4 to M6, may be accounted.

III. Calibration Technique and Simulation Results

An 8-bit DAC, with 8-bit calibration branches, has been simulated using the AMS08 technology and the TANNER tool. During the simulation, no mismatch error in the FETs and ideal connections between them have been assumed.

Fig.6 depicts the simulated INL of the proposed DAC, when the word 255 (0xFF) is employed as calibration word, for each branch. Despite the fact that no error sources (FET mismatch, wiring resistance) have been taken into consideration, the result can not be satisfactory (INL=2.4LSBits), since body effect of FET's, denoted as Q, introduces mismatches on their R_{ON}.

Apparently, the selection of the proper set of calibration words may lead to the improvement of DAC's linearity. The criterion for selecting the proper set of calibration words is based on the optimization of DAC's Signal-to-Noise Ratio (SNR), assigned as

$$\mathrm{SNR} = 10\log_{10}\left[\left(\frac{2^{N}-1}{2\sqrt{2}}\right)^{2} \Big/ \mathrm{Noise}^{2}_{\mathrm{RMS}}\right], \qquad (1)$$

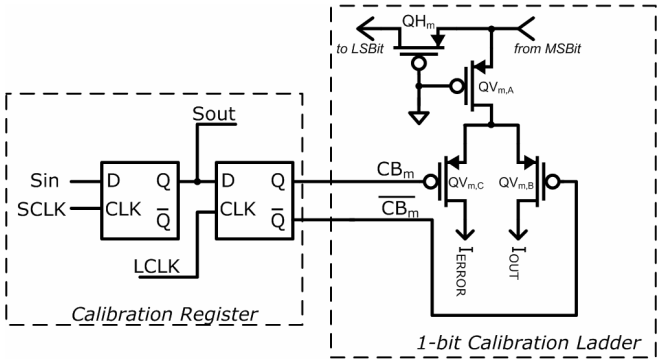

Figure 5. Internal architecture of a single bit of a calibration ladder.

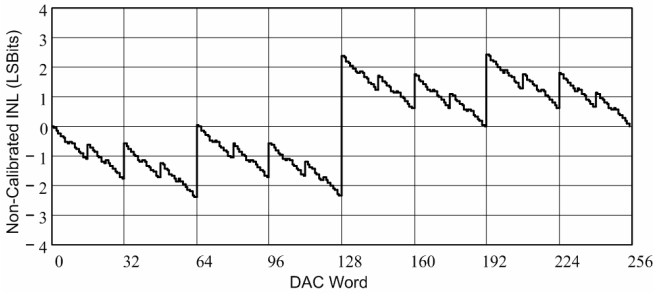

Figure 6. Simulated INL of the non-calibrated 8-bit ladder.

where $Noise_{RMS}^2$ is the RMS power of the quantization noise in $LSBits^2$ along with the noise introduced by DAC's non-linear effects, as shown in (2),

$$Noise_{RMS}^2 = \frac{1}{2^N - 1}\sum_{k=0}^{2^N-1}\int_{-1/2}^{1/2}\left(x + INL_k\right)^2 dx,\ LSBits^2. \qquad (2)$$

Eq. (2) denotes that the Noise RMS power can be directly connected with the INL produced for each DAC's word, as

$$Noise_{RMS}^2 = \frac{1}{12} + \frac{1}{2^N - 1}\sum_{k=0}^{2^N-1} INL_k^2,\ LSBits^2, \qquad (3)$$

where

$$INL_k = \left(2^N - 1\right)\frac{\left[I_{OUT(k)} - I_{OUT(0)}\right]}{I_{OUT\left(2^N-1\right)} - I_{OUT(0)}} - k,\ LSBits, \qquad (4)$$

assuming that $0 \le k \le 2^N-1$. Combining (1)-(4) SNR can be simplified as follows,

$$SNR = 10\log_{10}\left[\frac{\left(\frac{2^N-1}{2\sqrt{2}}\right)^2}{\frac{1}{12} + \frac{1}{2^N-1}\sum_{k=0}^{2^N-1} INL_k^2}\right]. \qquad (5)$$

Eq. (5) denotes that in order to maximize SNR, the INL's

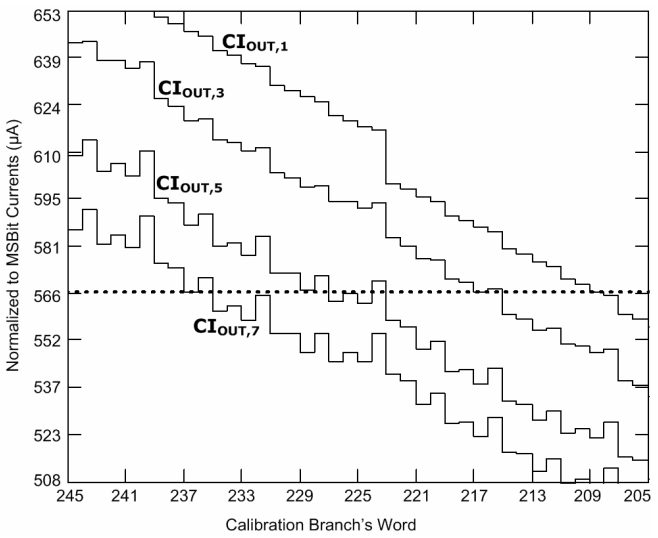

Figure 7. Normalized output currents of the calibration branches.

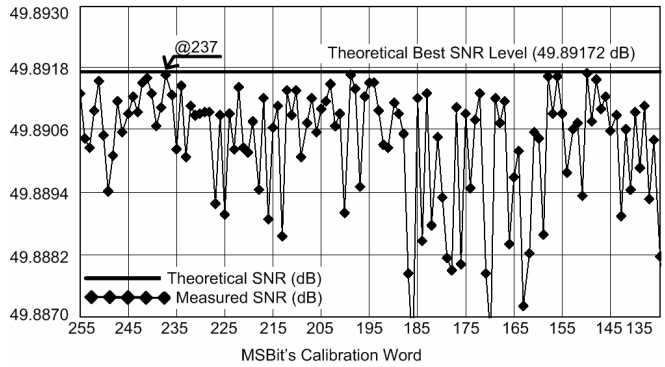

Figure 8. DAC's SNR as a function of the MSBit's calibration word.

noise power should be minimized, thus the least square algorithm should be applied for the corresponding INL, for each possible set of calibration words. Applying the above calibration algorithm, the output current of each calibration ladder has been measured. Fig.7 depicts, for means of clarity, only four out of eight, normalized to the MSBit, DAC bit currents, for a small range of calibration words (245-205).

Processing on these data has proved that, for each calibration word of the MSBit a specific SNR can be achieved, as depicted in Fig.8. TABLE I lists the 10-best SNR values achieved and the corresponding sets of calibration words. The selection of the proper set of calibration words can be easily performed, if the maximum current requirements are taken into account. After the calibration, the impact on the SNR of this selection is obviously negligible, as depicted in Fig.8. Therefore, the second row of TABLE I has been selected, while this selection is represented in Fig.7 as a dotted line. The derived INL, after applying the above calibration procedure, is depicted in Fig. 9.

Apparently, the INL of the calibrated DAC is significantly improved in comparison with the one depicted in Fig.6, as the maximum INL value has become less than 0.045 LSBits, while the corresponding SNR (49.891675 dB) can be considered as equal to the theoretical value (49.891716 dB). The goal of the presented architecture and its calibration procedure is that the optimization of the SNR is based on the DAC bits' currents trimming, according to calibration resolution (NC), regardless of FETs' R_{ON} mismatching; thus there always exist a 'most-proper' set of calibration words that leads to high linearity.

IV. Speed, Area and Power Characteristics

Speed performance of the proposed architecture can be considered identical to the one of the conventional current-mode R-2R ladder, as the current switching circuit, depicted in Fig.4,

TABLE I. Calibration words for 10-best SNR values.

SNR (dB)	Calibration Word							
	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
49.891716	*Theoretical best SNR level*							
49.891686	150	148	147	144	143	139	139	143
49.891675	**237**	**233**	**226**	**222**	**217**	**210**	**209**	**213**
49.891668	199	194	191	189	184	181	180	188
49.891645	156	155	153	151	149	144	144	149
49.891627	158	156	155	152	151	146	147	151
49.891619	241	236	235	226	222	216	215	218
49.891561	148	147	145	143	141	138	136	142
49.891549	251	247	243	236	231	224	223	227
49.891528	194	191	188	186	183	178	177	185
49.891520	195	190	189	184	182	177	176	184

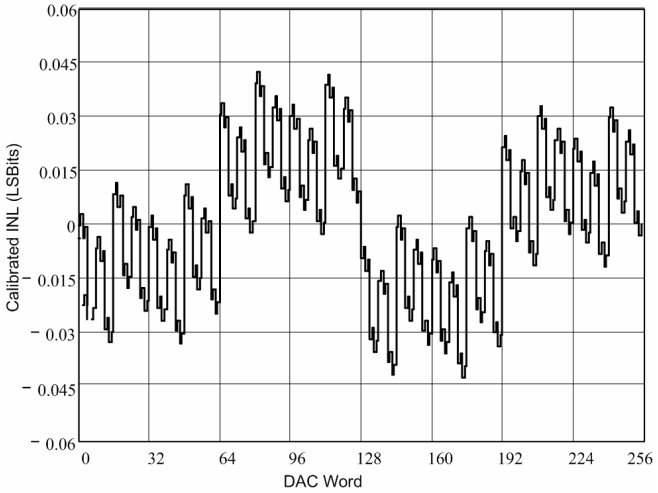

Figure 9. INL of the calibrated DAC.

employs a current cascode topology (FETs M4 to M6). Additionally, it should be emphasized that during the DAC operation all devices are in a steady state except the aforementioned FETs, which assign the output current.

The total device count of the proposed architecture can be compared with the one of advanced DAC architectures. Fig.10 compares the minimum device count required by a thermometer code or R-string DAC with the corresponding device count of the proposed architecture, assuming that NC=N.

The power consumption of the proposed architecture can be considered as at most double of the conventional current-mode R-2R ladder DAC. Taking into account Fig.1 and Fig.2 it can be found that the power consumed by a conventional ladder equals to $Vref \times I_{REF}$ while the proposed architecture requires this power for the biasing and additionally sinks the output current, thus increasing the total power consumption by $Vref \times I_{OUT}$. However, the maximum power consumption cannot exceed the $2 \times Vref \times I_{REF}$ value. Finally, it should be noticed that the extra digital logic, depicted in Fig.5 as calibration register, does not switch during the operation of the DAC, since it stores constant calibration words and thus does not contribute to the power dissipation.

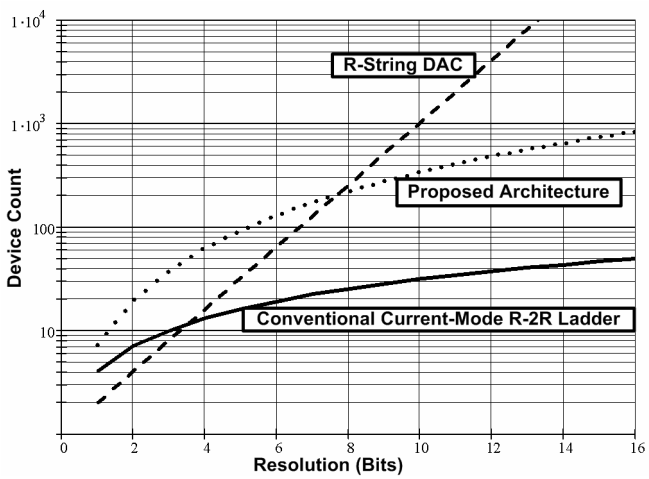

Figure 10. Device count comparison for 3-DAC architectures.

CONCLUSION

A current-mode, MOST-only, R-2R ladder-based, digitally calibrated DAC architecture has been presented in this paper. The architecture and circuitry of the DAC has been discussed in details along with a calibration algorithm, which is focused on obtaining the best SNR. The current trimming capabilities, derived by the proposed architecture, assign an inherent linear ladder-based DAC, as impacts of FETs' mismatching or any other error source's non-idealities are diminished.

Simulation results have certified the capabilities, of the proposed DAC architecture, in achieving high linearity. The proposed architecture minimizes the current and voltage switching, thus implying high speed along with low power characteristics. The implementation of the proposed DAC was based on standard CMOS technology and requires no special treatment for analog components, concluding in a low cost design.

ACKNOWLEDGMENT

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