An Analog PLL-based Technique for VCO Phase Noise Reduction

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Abstract—A PLL-based technique, able to reduce phase noise and non linearity of voltage controlled oscillators, is presented. According to this technique, the phase of a VCO can be sampled using an analog circuit (phase to voltage converter). The resulting signal is filtered and fed back to the VCO, decreasing its phase noise. Based on the phase/jitter properties extracted from transistor level analysis, a voltage domain behavioral model of the system was simulated and significant phase noise reduction was confirmed.

I. INTRODUCTION

Voltage-controlled oscillators (VCOs) constitute a critical component in modern communication systems. The specifications of wireless standards require tight performance for local oscillators, which cannot be met without several design tradeoffs. Phase noise is one of the most significant constraints, as there is a growing demand for higher number of channels and for better exploitation of the available bandwidth. Phase noise reduction comes at the cost of increased power consumption which limits the operating time of battery supplied wireless devices [1].

There are two main categories of oscillators, harmonic and relaxation. The first consist of an inductance-capacitance (LC) resonating circuit and a negative resistance active circuit used to compensate for the resonator losses [2]. Extensive studies of their noise mechanisms have led to optimized designs [3]-[6]. The used passive elements however, pose several constraints. The quality factor of on-chip spiral inductors is low and their dimensions are relatively large compared to transistors, resulting in increased power consumption and chip areas. Moreover, varactors, which give tunability to the circuit, are not able to provide wide tuning range.

Oscillators of the second category charge and discharge periodically a capacitor to produce the oscillating signal. Ring oscillators are the most representative topology of this category [7]. The delay of the inverters and the number of stages determine the oscillation frequency. Their disadvantage is the noise performance which is very poor for today's demanding applications in Gigahertz frequencies [6,8]. Nevertheless, their small chip area, the reduced power consumption and the wide tuning range [9,10] constitute attractive characteristics to designers.

This paper presents a technique able to reduce significantly the phase noise of any VCO type. According to this technique, a Frequency to Current Converter (FCC) is employed, embedding the frequency noise properties of the VCO output. The FCC's output current is integrated and thus, the output voltage of the integrator holds information regarding the VCO's phase noise. The integrator's output voltage is filtered and fed to the VCO's input. Since the control variable of this negative feedback loop is the phase, it can be considered as a Phase Locked Loop (PLL).

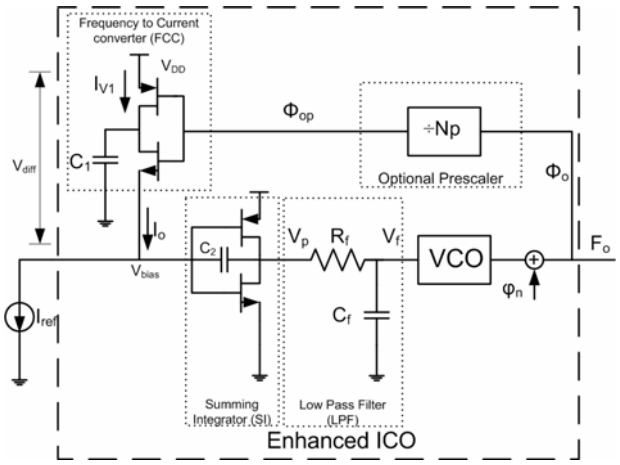

Figure 1. The proposed Current Controlled Oscillator.

The resulting closed loop system acts as a CCO (Current Controlled Oscillator) or VCO and has improved characteristics in terms of phase noise and linearity, employing a few analog elements. It is meaningful to apply this technique to a ring VCO since its main drawback, the phase noise, will drop significantly without affecting the rest of its properties.

The paper is organized as follows. Section II describes the operation of the system, its mathematical analysis and the noise characteristics. Section III discusses the simulation setup employed for the confirmation of the theoretical operation. In section IV, the simulation results are shown. Finally, design aspects and the conclusions are considered.

II. DESCRIPTION OF THE SYSTEM

Fig. 1 depicts the proposed system, which employs the noisy VCO with gain K_V (Hertz/Volt). The output frequency of the VCO, which can be optionally scaled down by a prescaler of ratio N_p, drives a simplified Frequency to Current Converter (FCC) that consists of an inverter with a small capacitance C_1 at its output. C_1 is charged at V_{DD} and discharged at V_{bias} on every cycle of the prescaler's output. Thus, the current I_o acquires the frequency properties of the output of the prescaler and consequently of the VCO. The average value of I_o is given by:

$$I_o(t) = \frac{F_o(t)}{N_p} V_{diff} \cdot C_1 \qquad (1)$$

where $V_{diff}=V_{DD}-V_{bias}$ and F_o is the VCO's output frequency.

The difference of I_o and the input current I_{ref} is integrated by the simplified Summing Integrator (SI) providing at its output a voltage that carries the properties of the integral of the VCO's output frequency, thus the properties of VCO's phase, as shown in the following expression:

$$V_P(t) = -\frac{1}{C_2}\int\left(\frac{F_o(t)}{N_p}V_{diff}\cdot C_1 - I_{ref}\right)dt \Rightarrow$$

$$V_P(t) = -\frac{C_1\cdot V_{diff}}{C_2\cdot N_p}\cdot\frac{\Phi_o(t)}{2\pi} + \int\frac{I_{ref}}{C_2}\cdot dt \quad (2)$$

It should be emphasized that the input voltage of the SI, V_{bias} remains constant since SI is a current summing integrator with negative feedback.

SI's output voltage is filtered by a simple low pass filter with $R_f C_f=T_f$, so as to reject any high frequency components and drives the VCO's input. Thus, a negative feedback, proportional to the VCO's phase feeds its input. The system is at steady state, when FCC's mean output current, given in (1), equals to the input current I_{ref}. This occurs when the output frequency is:

$$F_o = I_{ref}\frac{N_p}{C_1\cdot V_{diff}} = I_{ref}\cdot K_I \quad (3)$$

It becomes apparent that this system is a Current Controlled Oscillator (CCO) with a constant gain K_I (Hz/A) which does not depend on the gain K_V of the employed VCO. The system can also be analyzed in the frequency domain by rewriting (2), as:

$$V_p(s) = \frac{I_{ref}(s)}{sC_2} - \frac{C_1\cdot V_{diff}}{C_2\cdot N_p}\frac{\Phi_o(s)}{2\pi} \quad (4)$$

At the output of the VCO we have:

$$\Phi_o(s) = \frac{2\pi K_V}{s}\frac{1}{1+sT_f}V_p(s) \quad (5)$$

Substituting $V_p(s)$ in (5), we obtain the phase to current transfer function:

$$P(s) = \frac{\Phi_o(s)}{I_{ref}(s)} = \frac{2\pi}{s}\cdot\frac{N_p}{V_{diff}\cdot C_1}\cdot\frac{\omega_n^2}{s^2+2\zeta\omega_n s+\omega_n^2} \quad (6)$$

where:

$$\omega_n = \sqrt{\frac{V_{diff}\cdot K_V\cdot C_1}{N_p\cdot T_f\cdot C_2}} \quad (7)$$

and:

$$\zeta = \frac{1}{2\cdot\omega_n\cdot T_f} = \frac{1}{2\cdot\omega_n\cdot R_F\cdot C_F} \quad (8)$$

Consequently, the transfer function for the frequency is:

$$G(s) = \frac{F_o(s)}{I_{ref}(s)} = \frac{N_p}{V_{diff}\cdot C_1}\cdot\frac{\omega_n^2}{s^2+2\zeta\omega_n s+\omega_n^2} \quad (9)$$

Equation (9) confirms that the derived CCO has a gain K_I calculated in (3) and acts as a second order low pass filter with natural frequency ω_n and damping factor ζ.

The derived constant gain should be considered as a significant improvement since it contributes to the linear behavior of the system that employs this type of CCO. Additionally, its intrinsic low pass behavior is rather desirable in most of the real world applications. The natural frequency ω_n and the damping factor ζ can be adjusted so as to comply with the specifications and the requirements of the application where this CCO will be employed.

The key characteristic of the circuit is its ability to reduce significantly the in-band phase noise of the output frequency. The transfer function of the system with respect to the modeled phase noise Φ_n of the employed VCO is:

$$R(s) = \frac{\Phi_o(s)}{\Phi_n(s)} = \frac{s^2+2\zeta\omega_n s}{s^2+2\zeta\omega_n s+\omega_n^2} \quad (10)$$

implying that the VCO's phase noise is filtered by a second order high pass filter at ω_n and with damping factor ζ. Therefore, a phase noise reduction up to 40 dB per decade can be achieved in-band, for frequencies lower that the ω_n.

III. Simulation Setup

The circuit described above has been modeled and simulated in order to validate the theoretical results. The model was built using Verilog-A [14], an industry standard modeling language and the simulations were performed in Cadence environment. The process of predicting the jitter of the CCO system, with voltage domain models involves the following steps [11]:

- Use of SpectreRF [12] to predict the phase noise of the individual blocks that make up the CCO. These blocks are simulated in transistor level.
- Converting the phase noise of the individual blocks to jitter.
- Building high-level behavioral models for each block that exhibit jitter. This is established by dithering the time at which events occur. In this case the events are the zero crossings of the output signal.
- Assembling the blocks of the CCO into a general model.
- Simulating the CCO and sampling the zero crossings of the output signal.

After specifying the phase noise of each block in the second step of the previous process, the modeling requires

to convert it to jitter. This last term describes an undesired perturbation or uncertainty in the timing of events. There are several metrics of jitter. In the case of autonomous systems such as the VCO, the period jitter is used which is defined as the standard deviation of the length of a single period. Following the analysis in [11], the rms value of period jitter is given by:

$$J = \sqrt{cT} \tag{11}$$

where c is a quantity given in seconds and T is the oscillation period.

Oscillator phase noise is a variation in the phase of the oscillator as it proceeds along its limit cycle. It is the description of the jitter in the frequency domain. The most common metric of phase noise is the normalized single sideband power spectral density of the output voltage at a frequency offset Δf from the carrier, $\mathcal{L}(\Delta f)$, given in decibels below the carrier per Hertz (dbc/Hz) [6]. In [11], it is proven that:

$$\mathcal{L}(\Delta f) = \frac{c \cdot f_0^2}{\Delta f^2} \tag{12}$$

where f_0 is the oscillation frequency and Δf the frequency offset from the carrier.

Defining the phase noise specifications of the VCO, it is easy to extract the jitter information, using (11) and (12). Supposing an oscillator, operating at a frequency of f_0 =1GHz with $\mathcal{L}(\Delta f)$ = -140dbc/Hz at 20MHz offset, the rms period jitter equals 63 femtoseconds (fs).

Simulation results were derived by transient analysis for hundreds of microseconds and required several hours to complete since the simulator needs to capture the details caused by the jitter.

However this time is considered short, compared to the time required for the transistor level simulation, since Verilog-A [14] modeling is simple, accurate and time effective. The collected samples of the output signal zero crossings are post-processed in Matlab [15] in order to extract the closed-loop phase noise.

IV. Simulation Experiments

Simulations were performed for three setups of the CCO, varying the loop natural frequency and the damping factor. The results are taken for f_n=20MHz with ζ=0.5 and 0.7 and for f_n=40MHz with ζ=0.5. The desired performance of the circuit and the parameters of the employed components are listed in Tables I and II respectively. The capacitor at the output of the FCC is fixed to 200fF and the filter resistance to 500 Ohms.

One should notice that the selected natural frequency for the loop is high in contrast to classic PLL topologies where ω_n is in the range of KHz and is usually dictated by the reference frequency [13]. This is attributed to the fact that the applied frequency to the SI circuit, that samples the VCO's phase noise, can be equal even to its output frequency.

TABLE I. CCO Characteristics

Design parameters for the CCO	
Operating Frequency	1 GHz
VCO gain	1.2 GHz/V
Supply Voltage	3.3V
Ring VCO phase noise	-142 dbc/Hz@20MHz
Natural frequency	20 MHz, 40MHz
Prescaler ratio	4@f_n=20 MHz,2@f_n=40 MHz

TABLE II. Element Values

Passive elements			
System Variables (f_n, ζ)	20 MHz,0.5	20 MHz,0.7	40 MHz, 0.5
Capacitor C_1 (F to I)	200fF		
Capacitor C_2 (SI)	1.58pF	2.2pF	1.58 pF
Capacitor C_f(Filter)	15.9pF	11.4pF	7.95 pF
Resistance R_f	500 Ohm		

Figure 2 depicts simulation results for the VCO phase noise and the derived phase noise of the enhanced CCO for the values of ζ and ω_n mentioned above. The open-loop VCO presents a phase noise of -142dbc/Hz at 20MHz frequency offset. The simulation confirms the conclusions of the theory. The phase noise of the open loop VCO is high while the phase noise of the closed loop is kept flat inside the band. It is apparent that while the employed open loop VCO cannot be used for high performance applications, the derived CCO has significant better phase noise performance and can be compared directly to state of the art VCOs. [1,2,4].

Taking for example the GSM application, the specifications for the phase noise are listed in Table III. The numbers in parentheses indicate the difference between the devices' phase noise and the GSM standard. A VCO that has a phase noise of -142dbc/Hz at 20MHz offset, performs far away from the specifications. However, applying the proposed technique for a loop natural frequency of 20MHz for example, the phase noise level at 20MHz is maintained throughout the band below 20MHz, satisfying the demands of the specific standard. For f_n=40 MHz the closed-loop apparently performs better since the phase noise level at the specific frequency offset is lower.

TABLE III. Phase Noise Values

Phase noise (dBc/Hz)				
Offset frequency (Hz)	***GSM***	***VCO***	***CCO(f_n=20 MHz)***	***CCO(f_n=40MHz)***
100K	-112	-96 (+16)	-142 (-30)	-150 (-38)
600K	-126	-112 (+14)	-142 (-16)	-150 (-24)
3M	-142	-125 (+15)	-142 (0)	-150 (-8)

V. Design Considerations

The designer of the proposed CCO should take into account some important considerations concerning design and technical parameters of the system. First of all, the loop natural frequency ω_n should not exceed one tenth of the phase sampling frequency. This poses an upper limit in the selection of the loop frequency. The lower limit for ω_n is imposed by the VCO's phase noise at this frequency, which actually will be the highest phase noise level for the system. For example, for the specific VCO and the specific standard (GSM) the minimum value of f_n is 20 MHz.

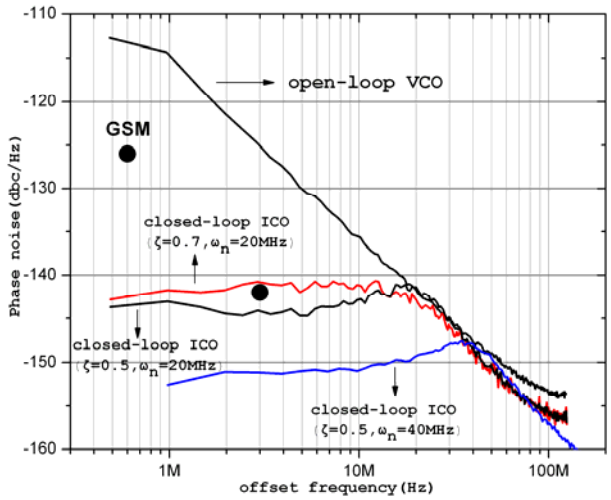

Figure 2. Phase noise of the closed-loop CCO at the output of the VCO when only the VCO exhibits jitter (closed-loop) for different values of damping factor and loop natural frequency versus the phase noise of the open loop VCO.

Moreover, it should be noted that the CCO gain K_I given in (3) is a very large quantity. As a result, attention should be paid to the design of the driving current source as it directly impacts the output phase noise below frequency ω_n. Alternatively, the use of a constant low noise current source will assign a non-zero free run frequency for the CCO, reducing at the same time the sensitivity of the system.

Additionally, Eqn. (3) implies that any fluctuations in V_{diff} will affect I_o and thus phase information. Therefore, the phase noise of the circuitry depicted in Fig. 1 suffers from V_{dd} fluctuation. However, a comprehensive circuit design, not presented here for sake of simplicity, could provide high immunity to this type of fluctuations.

VI. CONCLUSION

A PLL-based technique was presented, able to reduce by many decibels the phase noise of any VCO type. The implementation of the proposed technique requires a small number of additional elements and negligible power consumption overhead and, thus, it can be easily integrated. Moreover, it provides enhanced voltage to frequency linearity while retaining useful VCO characteristics, such as tuning range. However, the proposed system requires careful design regarding the noise of the low frequency components such as the input source and the integrator.

The proposed technique can be applied to today's high frequency demanding applications and especially in frequency synthesizers relaxing their design tradeoffs.

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