Instrumentation and Measurement
Technology Conference – IMTC 2007
Warsaw, Poland, May 1-3, 2007

An R-2R Ladder-Based Architecture for High Linearity DACs

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Abstract *– Digital to Analog Conversion performance is mainly characterized by its resolution, linearity and speed. Additional implementation characteristics include area and power dissipation. This paper presents a DAC architecture based on the conventional R-2R ladder topology that is able to derive a high-resolution, high-linearity and high-speed DAC, while requiring reasonable operating power and implementation area in a standard CMOS technology. Simulation results, derived both from numerical and circuit-level simulations, point out that the proposed architecture is able to derive any desirable resolution and linearity, without requiring low mismatch technologies or expensive trimming procedures.*

Keywords *– digital to analog conversion, resolution, linearity, settling time.*

I. INTRODUCTION

Nowadays signal processing typical requirements are increased, resulting to employment of digital rather than analog processing, since digital processing has better potentials. Consequently, signal conversion is mandatory, since more often than not the input and the output signals are analog. Signal conversion requirements continuously increase, in terms of conversion-speed, resolution, accuracy and power dissipation. Current technology for Digital-to-Analog Conversion (DAC) demonstrates techniques that achieve significant improvements regarding the aforementioned characteristics. However, several trade-offs prevent the design and implementation of a DAC, able to satisfy all the requirements.

DAC's linearity and resolution state-of-the art prescribe techniques such as $\Delta\Sigma$ conversion [1] and dynamically calibrated current sources [2], which however have poor conversion speed. On the other hand, ladder-based DACs [3] can offer high conversion speed, small area and power consumption, but they fail to comply with increased resolution and linearity requirements. Techniques able to approach high performance on speed, linearity and resolution, include thermometer code DACs [4], at the expense of area and power dissipation, or laser-trimmed [5] R-2R ladder-based DACs, using expensive manufactory procedures. The combination of the aforementioned techniques, derive hybrid DACs [6] or self-calibrated R-2R ladders [7], thus counterbalancing the strict requirements of the digital-to-analog conversion procedure.

This paper presents a DAC architecture based on the conventional ladder, able to fulfill tough requirements regarding resolution, linearity, conversion speed and power dissipation. Section II presents the proposed DAC architecture, section III presents circuit and numerical simulation results and finally, section IV proposes an innovative method for fast and accurate calibration of the proposed DAC.

II. ARCHITECTURE

Fig. 1 depicts the conventional current-mode R-2R ladder proposed by [8]. In this design, FETs labeled as QH_X represent the R resistances of the ladder, while the 2R branches are composed by the in series combination of FETs $QV_{X,A}$ and $QV_{X,B}$ or $QV_{X,C}$. All FETs are assumed of the same size, while active FETs operate at the linear region. The voltage difference Vref-Vbias is assumed small enough and thus body effect does not affect significantly the mismatching of the FETs' R_{ON}. However, the technology mismatch, along with the small difference in the voltage V_{SB} of the FETs, will indeed derive a mismatch on the FETs' R_{ON}, which bounds the linearity of the DAC.

The architecture proposed by [9] is based on the conventional R-2R ladder and is depicted in Fig. 2. In this architecture all FETs related to the R-2R topology are denoted as Q and are of the same size, while they operate at the linear region and have an R_{ON} resistance.

Each FET labeled as $QV_{X,B/C}$ in Fig. 1 has been replaced in Fig. 2 by an *NC*-bits ladder, acting as a bit calibration ladder, that is identical to the one depicted in Fig. 1, and a current mirror that mirrors the output current of each branch to the DAC's output according to the *NC*-bits digital input word of the specific bit calibration ladder. This replacement does not affect the R-2R topology benefits, since the input resistance of each calibration branch equals to one's FET R_{ON}. This modified topology enables the trimming of the output current of each calibration branch, according to the specific calibration word. Therefore, the modified topology offers the capability to trim each branch's current close-enough to the

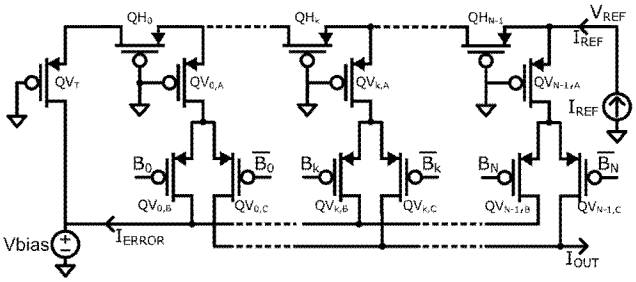

Fig. 1. Conventional CMOS-based R-2R ladder DAC.

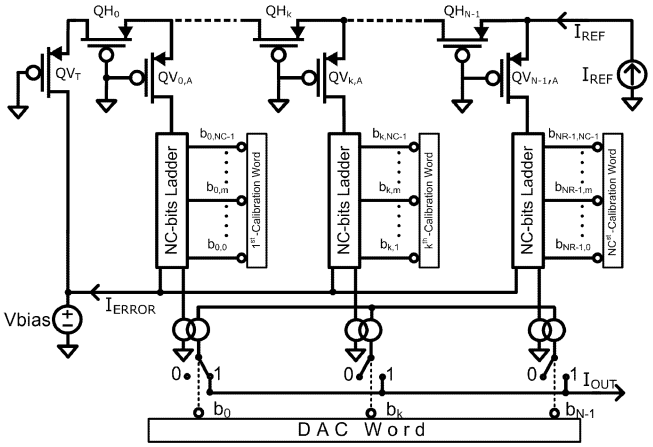

Fig. 2. The proposed architecture of the current mode DAC

optimum one. Apparently, the resolution of each calibration branch (*NC*) plays a major role, since it assigns the accuracy of the trimming procedure.

Fig. 3 denotes that the proposed ladder architecture can be synthesized by combining *NR* similar blocks, assuming that calibration words for each branch are settled using a simple serial interface. Each one of these blocks consists of the bit-calibration ladder and the DAC backbone (FETs QH_X, $QV_{X,A}$), as well as the required circuitry for current-cascading and the interface for assigning the calibration word. Digital signals Din, Dout, SCLK and LOAD are responsible for the assignment of the calibration word. Analog signals Cin and Cout are employed for the current-cascading, while CI_{OUT} is the output current of each block. Finally, the digital signal b_k represents the corresponding bit of the DAC's digital input word.

Each k-block of Fig. 3 (k=0…*NR*-1), depicted in more details in Fig. 4, consists of a single element of the DAC backbone (QH_k and $QV_{k,A}$). Each calibration branch is composed by *NC*-similar blocks, one for each calibration bit, and a current mirror (FETs M1 to M4), that mirrors the branch's output current to the output node, while the error current is let to the ground (through FETs E1 and E2) and FETs S1 and S2 switch the bit's current to the ladder's output.

Finally, each block $CBit_m$ (m=0…*NC*-1),, representing a calibration bit, depicted in Fig. 4, consists of one bit calibration register and a single bit calibration ladder, as depicted in Fig. 5. Calibration register consists of two D-FF's and enables the serial-input/ parallel-load of the DAC's calibration words. The single bit calibration ladder is identical to the cell of the ladder as depicted in Fig. 1.

As soon as the calibration words have been assigned, all

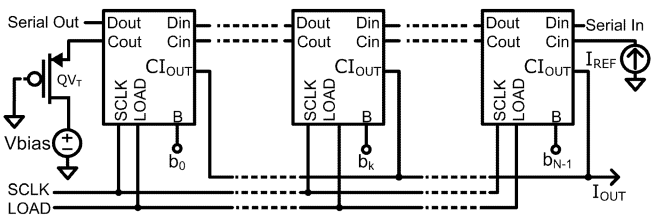

Fig. 3. Block diagram of the proposed DAC circuitry.

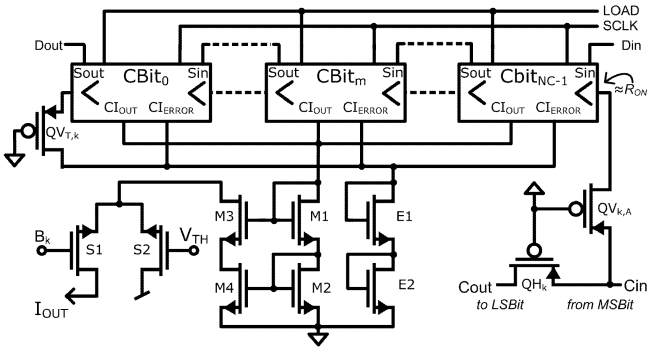

Fig. 4. Internal architecture of a ladder's block.

FETs, labeled as Q, M and E operate at a steady-state, regardless of the DAC's digital input. Only FETs S1 and S2, of each calibration branch, alternate their operating conditions according to the DAC word. This implies that most of the circuitry operates in constant bias conditions, as only a small portion of it has to switch, thus contributing to high speed performance. Since current, in most FETs, is constant, the power consumption of the circuit will be approximately close to $2\times VDD\times I_{REF}$.

III. SIMULATION RESULTS

The proposed architecture has been simulated both numerically, employing Matlab for studying the DAC's behavior over a wide range of cases regarding the resolution and the resistors' mismatch, and at circuit level, employing Tanner circuit simulator on an 8-bits DAC with 8-bits calibration branches, implemented using a standard CMOS technology.

A. Numerical Simulation

Numerical simulations, covering a wide range of resolutions (*NR*=4-16) and calibration lengths (*NC*=1-16), for a wide range of components' mismatches (m_e=0.1%-10%) have been performed using Matlab.

Fig. 6 presents the estimated mean linearity (INL) of a ladder employing components of constant mismatch (m_e=0.01 or 1%), for a range of resolutions (*NR*=8-15) and calibration lengths (*NC*=1-16). Apparently, the more calibration length is increased, the more the DAC's linearity gets improved, since the current trimming capabilities are exponentially increased.

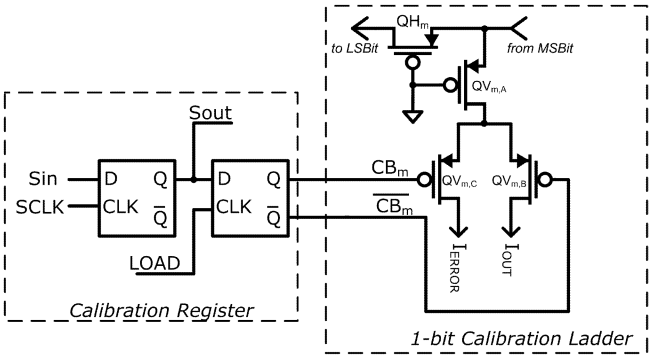

Fig. 5. Internal architecture of a single bit of a calibration ladder.

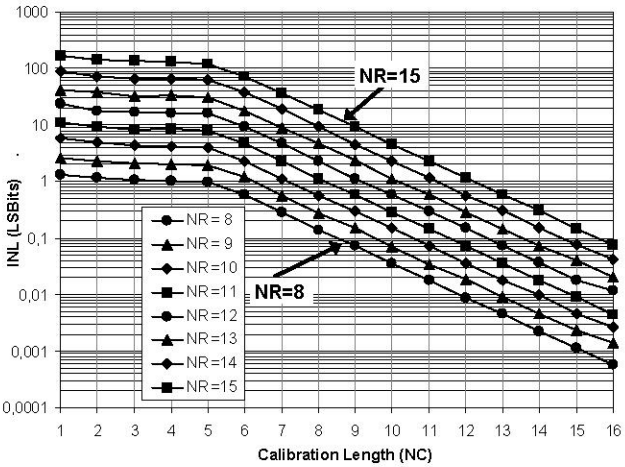

Fig. 6. Simulated INL mean value for mismatch me=0.01 (1%) for various resolutions.

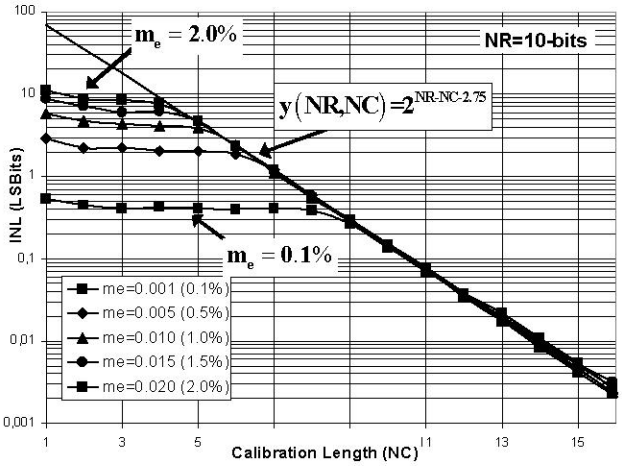

Fig. 7. Simulated INL mean value for 10-bits resolution at various mismatches.

However, for small values of calibration length (NC<5 for m_e=1%) no linearity improvement can be considered, which is reasonable, since calibration branches do not have the adequate resolution in order to trim the current contribution of each bit.

Fig. 7 presents the estimated mean INL for a certain ladder's resolution (NR=10), employing components of a wide range of mismatches (m_e=0.1%-2%) and for a wide range of calibration lengths (NC=1-16). The pattern of these simulated results leads to a twofold approach, regarding the calibration length NC:

- When calibration length NC is small, the proposed architecture does not improve DAC's linearity, which has a certain value that depends only on the DAC's resolution NR and the components' mismatch m_e.
- When calibration length NC is adequate, the ladder's linearity depends on the DAC's resolution NR and the calibration length NC while does not depend on the components' mismatch m_e.

This indicates that the proposed architecture is able to provide high-resolution, high-linearity ladders, with out requiring advanced technology, in terms of components' mismatch. Equation (1) is the empirical formula that fits on the horizontal lines of Fig. 6 and Fig. 7, thus in the region where the proposed architecture cannot achieve linearity improvement. Therefore, (1) gives the estimated mean INL value of the conventional ladder as a function of its resolution, NR, and the mismatch, m_e, of the employed components,

$$\overline{\mathrm{INL}}(m_e, NR) = 0.577 \cdot m_e \cdot 2^{NR}(LSBits) \qquad (1)$$

Equation (2) is the empirical formula that fits on the diagonal line of Fig. 7 and derives the estimated mean INL value of the proposed ladder, as a function of the resolution and the calibration length NC,

$$\overline{\mathrm{INL}}(NR, NC) = 2^{NR-NC-2.25}(LSBits) \qquad (2)$$

According to the simulation results, the proposed ladder architecture is able to derive a linear DAC of any resolution, regardless of the technology mismatch. Equation (2) implies that designing a ladder with calibration length equal to the resolution length minus two (NR-2) will produce a DAC with mean INL value less than one. Further statistical analysis on the simulation results pointed out that when NC equals to NR-1, the maximum derived INL would always be less than 1-LSBit, regardless the technology's mismatch. Apparently, this is a significant conclusion, since it implies that the proposed architecture is able to implement high-resolution, high-linearity and high-speed D/A converters employing a simple methodology on a standard CMOS technology.

B. Circuit simulation

An 8-bits DAC, with 8-bits calibration branches, has been simulated using the AMS08 technology and the Tanner tool. During the simulation, zero mismatch error for the FETs' size and ideal connections between them has been assumed. Despite this, circuit simulation derives an INL of 5-LSBits if employing the word 255 (0xFF) as the calibration word for all branches, thus concluding to an un-calibrated DAC.

Calibration procedure requires the adjustment of the calibration words, so as each bit to contribute with a current value as close as possible to the ideal one. For each calibration word of the MSBit, a set of calibration words for the rest bits of the DAC that derive the minimum INL can be found.

As Fig. 8 denotes, there are many sets of calibration words, one set for each calibration word of the MSBranch; however, one set would provide the best results. Employing the aforementioned calibration algorithm, the best INL (0.054-LSBits) achieved by setting the value 237 (0xED) as the calibration word for the MSBit. However, it should be emphasized that, as it can be seen in Fig. 8, for any calibration word of the MSBit, in the range 255-192 (0xFF-0xC0), the worst INL achieved was less than 0.5-LSBits. Additionally it should be emphasized that according

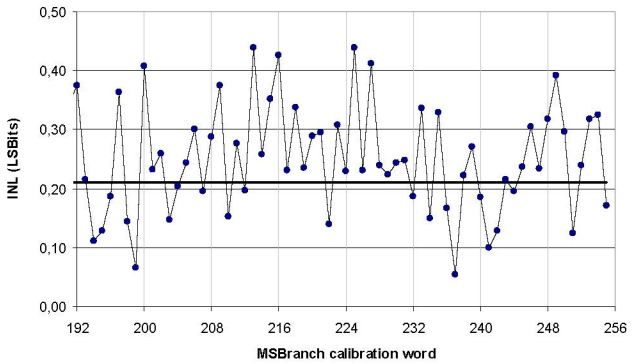

Fig. 8. INL achieved for a range of calibration words for the MSBranch.

to the empirical formula (2), derived by the numerical simulations, the estimated mean INL for this DAC is $2^{-2.25} \approx 0.21$, which is in accordance to the achieved INL value.

The current switching time for any possible transition did not exceeded the 20ns, a time that can be considered as more than satisfactory for the employed technology.

IV. CALIBRATION

Calibration of the proposed ladder demands the estimation of the proper calibration word, for each branch, so as to equalize their normalized currents. The first step is to calculate the normalized current for each branch and for each calibration word. The second step requires finding for each possible calibration word, of the MSB branch, the nearest normalized currents of the rest branches, and calculating the error matching, by applying the least square algorithm. Finally, the best linearity will be achieved by applying the set of calibration words that provides the minimum error. However, if applying any other set of calibration words derived by the calibration algorithm, a DAC with significantly improved linearity characteristics will be obtained in comparison to the conventional R-2R ladder.

In real world, the calibration of a ladder, based on the proposed architecture, cannot be easily performed by following the aforementioned calibration procedure, applied for the simulation, since it is not easy to accurate measure all the currents.

An elegant calibration method, based on the properties of an alternative phase detector, designed towards to PLL-based frequency synthesis is presented in [10], and can be employed to facilitate and accelerate the calibration of the proposed ladder. This phase detector, named as "Dual Input Phase Accumulator" (DIPA), derives at its output the phase difference of two non-equal frequencies F_1 and F_2 by applying a normalization technique. DIPA consists of a digital portion that implements the required function and a DAC for generating the analog output corresponding to the normalized phase difference. Additional to the two inputs for the frequencies F_1 and F_2, DIPA employs two more digital inputs W_1 and W_2 where the phase normalization factors are applied. DIPA's proper operation requires applying on W_1 a value proportional to the frequency applied on input F_2 and

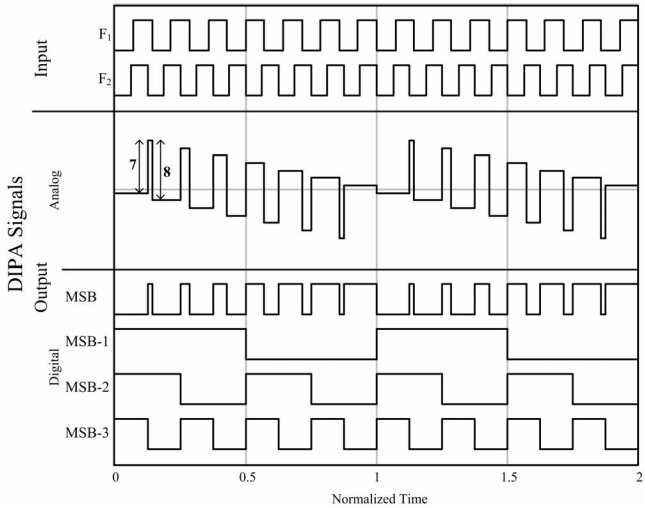

Fig. 9. DIPA's input/output analog/digital signals.

consequently, a value proportional to the frequency F_1 should be applied at input W_2.

An example that demonstrates the operation of a 4-bits DIPA (*NR*=4) is depicted in Fig. 9, assuming that two frequencies with normalized values F_1=7 and F_2=8 are applied on its two inputs. On each falling edge of F_1 the analog output of the DIPA is decreased by W_1=8, while on each edge of F_2 is increased by W_2=7. Thus, DIPA's output mean value remains constant, indicating that the normalized phase difference of the two input frequencies is constant. It has been proven in [10] that DIPA's AC output current in this example can be expressed in Fourier series as shown in (3),

$$I_{DIPA}(t)=\frac{W_2 I_{FS}}{2^{NR}\pi}\sum_{i=1}^{\infty}\frac{1}{i}\sin(2\pi i F_2 t)-\frac{W_1 I_{FS}}{2^{NR}\pi}\sum_{i=1}^{\infty}\frac{1}{i}\sin(2\pi i F_1 t), \quad (3)$$

where I_{FS} is the full scale output current of the DAC.

Apparently, DIPA's output signal consists of harmonics of the two input frequencies on the condition that the employed DAC is ideal. Observing, in Fig. 9, the digital waveforms that drive DIPA's DAC, it is easy to conclude that a mismatch error between the current contributions of MSB and MSB-k will superimpose to the ideal output, a square waveform with a frequency 2^{k-1}-times the beat frequency of F_1 and F_2 ($F_b=|F_2-F_1|$) and an amplitude Ierr(k) proportional to the aforementioned mismatch error:

$$Ierr(k)=I_{MSB\text{-}k}-\frac{I_{MSB}}{2^k} \quad (4)$$

and is expressed in time domain employing Fourier series as:

$$Ierr(k,t)=\frac{2}{\pi}\left(I_{MSB\text{-}k}-\frac{I_{MSB}}{2^k}\right)\sum_{i=1,3,5...}\frac{1}{i}\sin\left(2^k\pi i F_b t\right). \quad (5)$$

Apparently, in the case of employing a non-ideal DAC, DIPA's output will include harmonics of the beat frequency, thus low frequencies. It is noticeable that, in the example

depicted in Fig. 9, the amplitude of 1st, 2nd and 4th harmonic of the beat frequency that will appear at DIPA's output will be directly proportional to the mismatch error between the analog contribution of the MSB and MSB-1, MSB-2 and MSB-3 respectively. By measuring the amplitude of the aforementioned harmonics of the beat frequency, the mismatch errors of the corresponding bits could be easily calculated by multiplying these amplitudes with $\pi/2$. The phase of these harmonic point out the sign of the amplitude, thus indicate if the current contribution of a bit is more or less the ideal value.

For calibrating MSB-1, 2 and MSB-3 bits of a DAC it is required to minimize the corresponding errors, thus to set the calibration words that minimize the 1st, 2nd and 4th harmonic of the beat frequency.

A simple strategy for calibrating rest least significant bits of a multi-bits DAC, assumes as MSB the already calibrated MSB-k (k=1…*NR*-1) and requires shifting DIPA's 4-bits digital output bus down on the least significant, uncalibrated bits of DAC's input bus. Then the same calibration procedure is applied, assuming MSBits already calibrated. This simplified calibration procedure requires reduced infrastructure in terms of hardware (4-bits DIPA) and instrumentation (low frequency resolution spectrum analyzer), however may not conclude to the best calibration, since reference current is not unique.

In order to achieve the best calibration results for a multi-bits DAC, also a multi-bits DIPA should be employed so as to drive simultaneously all the DAC bits. Assuming that an *NR*-bits DAC has to be calibrated also an *NR*-bits DIPA should be employed. The ratio of the two input frequencies F_1/F_2 should be assigned to be $(2^{NR-1}-1)/(2^{NR-1})$ and phase-normalizing input words to the DIPA should be $W_1=2^{NR-1}$ and $W_2=2^{NR-1}-1$ respectively. In this case, calibration procedure requires minimizing the amplitudes of *NR*-1 specific harmonics of the beat frequency F_b located at frequencies $2^{k-1}F_b$ ($1 \le k \le NR-1$). Based on (5), a formula that assigns DIPA's harmonic contents due to the DAC's non-linearity can be found:

$$\mathrm{Ierr}(t)=\sum_{k=1}^{NR-1}\left(\frac{2^k I_{MSB-k}-I_{MSB}}{2^{k-1}\pi}\sum_{i=1,3,5\ldots}\frac{1}{i}\sin\left(2^k\pi i F_b t\right)\right) \qquad (6)$$

According to the above formula DAC's non-linearity generates harmonics of the beat frequency F_b. Further investigation on this formula discloses that bandwidth below frequencies F_1 and F_2 is filled-up with harmonics of F_b. Each one of these harmonics is generated due to a single bit mismatch, however the first and consequently the strongest harmonic of MSB-k bit is located at frequency $2^{k-1}F_b$ ($1 \le k \le NR-1$). This is a significant property of the DIPA since it facilitates the accurate measurement of the mismatch contribution of each bit of the DAC, and consequently its accurate, fast and easy calibration. DIPA based calibration procedure has been confirmed by numerical simulations using Matlab.

In system calibration of the proposed architecture DAC is also an option. Since the performance of a system is affected by the linearity of the employed DAC, it can be calibrated using as criterion the improvement of the system's performance.

V. CONCLUSION

A current-mode, MOST-only, R-2R ladder-based, digitally calibrated DAC architecture has been presented in this paper. The architecture and circuitry of the DAC has been discussed in details along with the properties that affect the linearity, the conversion speed and the power dissipation. The implementation of the proposed DAC was based on standard CMOS technology and requires no special treatment for the analog components regarding the mismatch error, concluding in a low cost design. Simulation results have certified the capabilities of the proposed DAC architecture, in achieving high linearity. Moreover, empirical formulas have been derived, interpreting the design properties of the ladder as a function of its desired linearity. Finally, an innovative method for accurately measuring the contribution of each DAC's bit to the overall DAC's non-linearity has been proposed, aiming to simplify and accelerate the calibration procedure of the proposed ladder.

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