Linear Range Extension of a Phase-Frequency-Detector with Saturated Output

Michail Papamichail, Dimitrios Karadimas, Konstantinos Efstathiou and George Papadopoulos
Department of Electrical and Computer Engineering, University of Patras
Rion Campus, 26500, Patras, Greece
mpapamicha@apel.ee.upatras.gr

***Abstract*—A Phase Frequency Detector (PFD) with wide linear operating range and the ability to saturate beyond that range is presented in this paper. Its use in phase locked loops (PLLs) implies elimination of cycle slipping, which results in an analytically predictable transient behavior and a possible improvement in acquisition speed, depending on the PLL design. Simulation results confirm these advantages. Moreover, a detailed study on the applicability of this PFD is conducted in this paper.**

I. Introduction

The Phase Detector (PD) constitutes a critical component of Phase Locked Loops (PLLs). The PD having prevailed in PLL applications is the Phase Frequency Detector (PFD). However, limitations in the width of its linear operating range, which occasionally have impact on the acquisition speed of the PLL, have encouraged many designers to propose PDs that present superior properties. The accumulative PD proposed in [8], for example, achieves wider linear operating range at the cost of a significant circuitry increase. Most other techniques aim to improve acquisition speed and employ nonlinear PDs, or adaptive PDs that control the gain or the bandwidth of the loop [9,10,11,12]. In [9] a more detailed survey of these techniques can be found.

This paper proposes a PD based on the conventional PFD, modified so as to obtain wide linear operating range, while at the same time eliminating the cycle slipping effect. Employing the proposed PFD in a PLL improves the acquisition speed in wide transients, without affecting its operation in steady state.

Section II of this paper studies the limitations of the conventional PFD. Section III presents the proposed PFD architecture and its operation. Section IV studies the proposed PFD properties and applications and, finally, Section V summarizes the results.

II. Conventional PFD - Limitations

Conventional PFD (C-PFD) is a sequential logic circuit which detects the phase difference of two signals, while at the same time provides a frequency sensitive signal aiding acquisition when the loop is out of lock. A simple implementation of PFD and its state transition diagram (STD) are shown in Figure 1 (a) and (b).

The digital outputs of the PFD are converted into analog quantity by using a charge pump, and are then passed through the PLL's loop filter that drives the VCO. The transfer characteristic of C-PFD is illustrated in Figure 1 (c).

It can be seen that the range of linear operation is ideally $\pm 2\pi$. For greater phase difference between the input signals PFD behaves nonlinearly, a fact that deteriorates the acquisition process of the loop. Figure 2 depicts a simulation example of the acquisition process of a PLL, where the phase difference of the two input signals exceeds 2π. As it can be seen, at time $\omega_n t_{2\pi}=1.111$ a cycle slipping occurs and the response of the loop diverges from the expected.

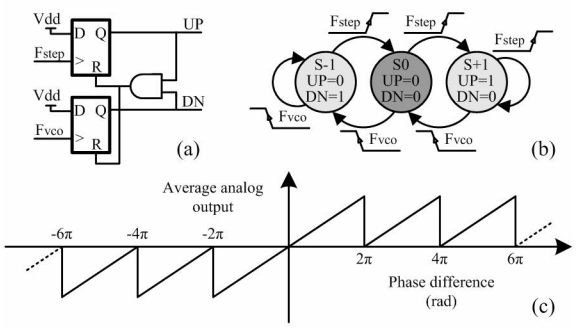

Figure 1. Conventional PFD. (a) Circuit implementation, (b) State Transition Diagram, (c) Transfer characteristic.

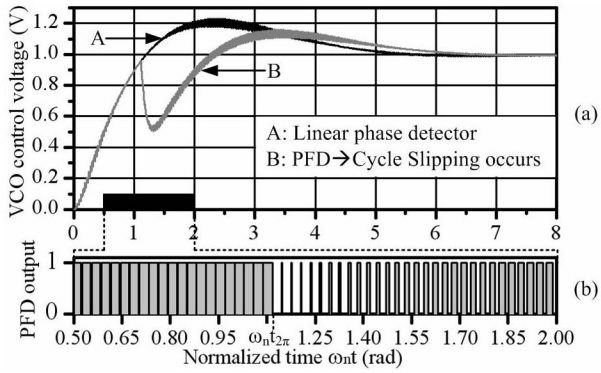

Figure 2. Transient behavior of a PLL upon a frequecy step. (a) VCO control voltage (Lowpass filtered), (b) PFD output (zoomed): at $\omega_n t_{2\pi}$ the duty cycle erroneously resets to zero.

Cycle slips in general impose a more sluggish transient behaviour to the PLL, which cannot be analytically predicted with linear techniques. The implications become more severe as the frequency step increases or the natural frequency of the loop (ω_n) decreases or the damping factor (ζ) decreases.

III. The Proposed PD Architecture

As is established in section II, cycle slipping of C-PFD deteriorates the acquisition process of the PLL. A PD with a transfer characteristic that saturates for phase errors be-

yond ±2π, as the one depicted in Figure 3 (a), could improve the acquisition speed by eliminating cycle slips. When phase error exceeds ±2π, such a PD, the saturated PFD (S-PFD), drives the loop filter with the maximum output, thus forces VCO to converge to the proper frequency with the maximum speed. Figure 3 (b) illustrates the state transition diagram (STD) of S-PFD. However, in the case of S-PFD the transient behaviour of the PLL cannot still be expressed in a closed form.

It is apparent that a linear transfer characteristic exceeding the ±2π limitation would further increase the acquisition speed in wide frequency steps, making at the same time the behavior of the loop predictable. Figure 4 (a) illustrates the transfer characteristic of such a phase detector that is able to operate linearly in a range of ±2nπ, while exhibiting saturation beyond this range. The STD of this Wide-range Saturated PFD (WS-PFD) is shown in Figure 4 (b).

The operation of the STDs depicted in Figure 3 (b) and Figure 4 (b), is quite simple and is based on accumulating UP/DN levels according to the count of the edges of the Fstep/Fvco signals, i.e. on each edge of Fstep/Fvco the count of UP/DN increases by one or the count of DN/UP decreases by one, depending on the current state of the STD. Notation UP=0 means that all UP outputs equal zero, while notation UP^n=1 means UP1=UP2=…=UPn=1.

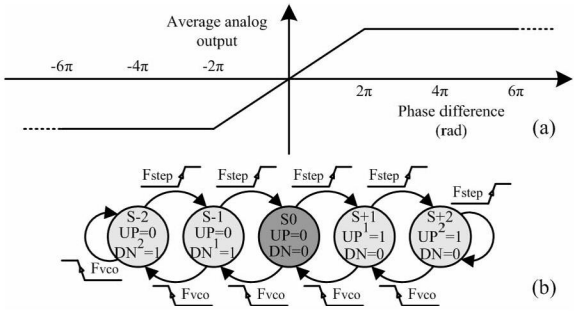

Figure 3. Saturated-PFD. (a) Transfer characteristic, (b) State Transition Diagram.

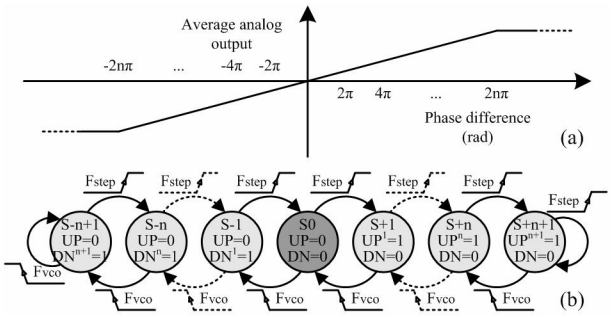

Figure 4. n-level Wide-range Saturated-PFD. (a) Transfer characteristic, (b) State Transition Diagram.

The implementation of the above STDs can be simplified by using the two cells depicted in Figure 5 (a) and (b), while the block diagrams of S-PFD and n-level WS-PFD are depicted in Figure 5 (c) and (d) respectively. The charge pump of the proposed PD is identical to the C-PFD's one. Each UP/DN output drives an equally sized pmos/nmos current source that sources/sinks a predefined amount of current. It should be denoted that WS-PFD's (S-PFD's) outputs UPn+1, DNn+1 (UP2, DN2) are ignored in order to obtain saturation. Additionally, it should be emphasized that in the phase locked condition, or generally for phase differences less than ±2π, the active states are S0, S+1, S-1 and the operation of S-PFD and WS-PFD is identical to that of C-PFD. Therefore, the power consumption of the proposed PFDs can be considered almost the same as the C-PFD's one, since the additional circuitry is inactive during the locked state. Moreover, the dead zone issue appears only during the locked state and thus, design techniques for the C-PFD that handle this problem can be applied to the proposed PFDs as well.

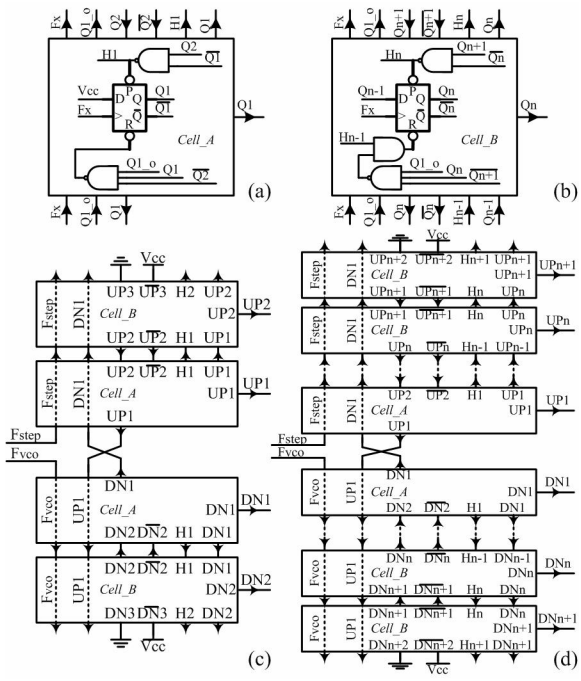

Figure 5. Circuit implementation of the proposed phase detectors. (a) Cell_A, (b) Cell_B, (c) S-PFD, (d) n-level WS-PFD.

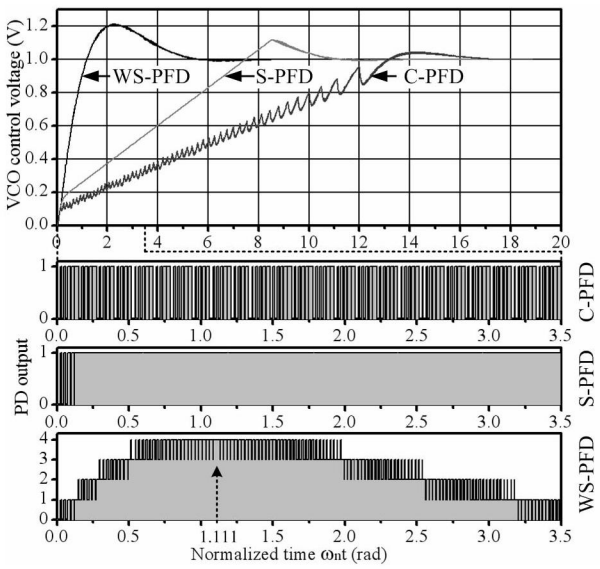

Figure 6. Transient response of a PLL for three different PDs. (The response of the PDs is zoomed)

The transient response of a PLL incorporating C,S-PFDs and a 4 level WS-PFD, all with identical K_d gains, was simulated using Matlab. A type-II, second-order PLL with ω_n=2π1000 rad/sec and ζ=0.707 was tested. Figure 6

shows the transient response for a frequency step input of Δf=55.123kHz ($f_{vco_free_run}$=200kHz, f_{step}=255.123kHz) for the three types of PFDs. It is clear that no cycle slipping occurs when S-PFD is used as the phase detector, resulting to a 57% faster settling than the C-PFD's one. Regarding to WS-PFD, which does not saturate, it is clear that it presents a typical type II second order step response.

Since the transfer function, and thus ω_n and ζ, are the same for all PLLs, there is no obvious penalty of phase noise. Indeed, the phase noise power spectral density $S_\varphi(f)$, as is given in [3], is the same for PLLs with the same transfer function and the same VCO gain K_O, i.e. the noise coming from the VCO, the reference, the loop filter and the feedback divider remains the same. In [4], the noise contribution due to the phase detector is also considered, and is found to increase for lower PD gain. Unless it is not possible to use a greater value for the full scale current than the one used in C-PFD, the noise due to the PD will not change either.

IV. Applications of the Proposed PFDs

Incorporation of S-PFD or WS-PFD in a PLL experiencing frequency steps is of advantage when the transient behavior of the loop suffers from cycle slipping. In order to find out which PLL designs could benefit from the proposed phase detector architecture we have to investigate the behavior of the maximum phase error developed during the acquisition process upon the width of the frequency step and upon physical quantities of the loop such as the natural frequency (ω_n) and the damping factor (ζ). For all those PLL applications where the maximum phase error exceeds $\pm 2\pi$ during frequency steps, use of the proposed phase detector seems to be beneficial.

For the purposes of the analysis, a second order PLL having the transfer function in (1) will be considered.

$$H(s) = \frac{2\zeta\omega_n s + \omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \tag{1}$$

This is the transfer function of PLLs with voltage output PD that use active PI filter [1, 2] and of PLLs with current output PD that use first order passive RC filter [1]. It is also approximately the transfer function of most practical high gain second order PLLs with voltage output PD [2]. The error transfer function is shown in (2).

$$H_e(s) = \frac{s^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \tag{2}$$

For a frequency step $\Delta\omega$ applied to the input at $t=0$, the phase error signal is given in Laplace form in (3) [2].

$$\Theta_e(s) = \frac{s^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \cdot \frac{\Delta\omega}{s^2} \tag{3}$$

Applying the inverse Laplace transform to (3) we derive the phase error signal in time domain, given in (4) for $\zeta \neq 1$.

$$\vartheta_e(t) = \Delta\omega \cdot \frac{e^{-\zeta\omega_n t}}{\omega_n\sqrt{1-\zeta^2}} \cdot \sin(\omega_n\sqrt{1-\zeta^2}\,t) \tag{4}$$

The time where the maximum phase error occurs can be found by solving the equation $d\theta_e(t)/dt=0$ and is given in (5). This time depends only on ω_n and ζ.

$$t_{\max}(\omega_n,\zeta) = \frac{\arctan\left(\frac{\sqrt{1-\zeta^2}}{\zeta}\right)}{\omega_n\sqrt{1-\zeta^2}} \tag{5}$$

Evaluating $\theta_e(t)$ at t_{max}, the maximum phase error θ_{e_MAX} as a function of $\Delta\omega$, ω_n and ζ, is derived:

$$\vartheta_{e_MAX}(\Delta\omega,\omega_n,\zeta) = \frac{\Delta\omega}{\omega_n} \cdot \frac{e^{\frac{\arctan\left(\frac{-\sqrt{1-\zeta^2}}{\zeta}\right)}{\frac{\sqrt{1-\zeta^2}}{\zeta}}}}{\sqrt{1-\zeta^2}} \cdot \sin\left(\arctan\left(\frac{\sqrt{1-\zeta^2}}{\zeta}\right)\right) \tag{6}$$

Which can be simplified to:

$$\vartheta_{e_MAX}(\Delta\omega,\omega_n,\zeta) = \frac{\Delta\omega}{\omega_n} \cdot C(\zeta) \tag{7}$$

Or it can be approximated to:

$$\vartheta_{e_MAX}(\Delta\omega,\omega_n,\zeta) \cong \frac{\Delta\omega}{\omega_n} \cdot \frac{1}{1.767\cdot\zeta + 0.960} \quad \textit{for } \zeta \textit{ in } (0,1.5] \tag{8}$$

Figure 7 illustrates the PLL's cycle slipping free operating areas for several levels of WS-PFDs. The area under any curve constitutes the locus of the operating points of the PLL in which it is safe to use a phase detector with a $\pm 2n\pi$ rad linear range without experiencing cycle slipping.

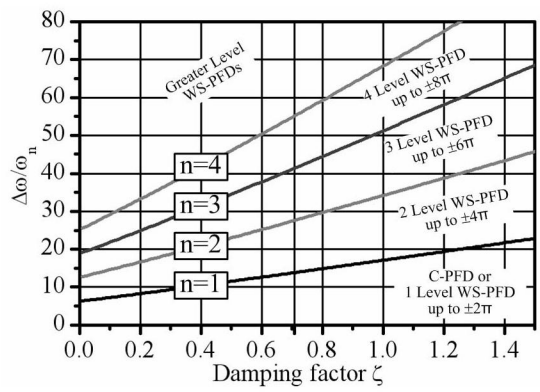

Figure 7. Cycle slipping free operational areas of a PLL with various PFDs.

In order to verify the results, we consider the PLL simulation in Figure 6, where $\Delta\omega/\omega_n=55.123$ (actually just over 55.123) and $\zeta=0.707$. According to Figure 7, a 4 level WS-PFD is marginally adequate. Indeed, in the simulation in Figure 6, we can see that at $\omega_n t$=1.111 the phase detector output saturates for one cycle (pointed by an arrow) because the phase difference marginally exceeds 8π. Fur-

thermore, for $\zeta=0.707$ (5) gives normalized time that equals 1.111.

In the case of an Integer N frequency synthesizer, the feedback loop incorporates a frequency divider with divisor values in the region [N_{min}, N_{max}]. The maximum frequency difference in the phase detector inputs is observed during the F_{max} to F_{min} transition and is equal to $(F_{max} - F_{min})/N_{min}$. Substituting this difference in (7) and setting $\theta_{e_MAX}=2n\pi$ we derive (9).

$$\frac{2\cdot\pi\cdot\frac{F_{\max}-F_{\min}}{N_{\min}}}{2\cdot\pi\cdot f_n}=\frac{2\cdot n\cdot\pi}{C(\zeta)} \tag{9}$$

Taking into account that $f_{step}=F_{min}/N_{min}$ we derive (10) which is plotted in Figure 8 for $\omega_n/\omega_{step}=1/100$ and various values of n.

$$\frac{F_{\max}}{F_{\min}}(\zeta)=\frac{2\cdot n\cdot\pi}{C(\zeta)}\cdot\frac{f_n}{f_{step}}+1 \tag{10}$$

Every curve denotes the maximum F_{max}/F_{min} ratio of a synthesizer incorporating an n-level WS-PFD that ensures cycle slipping free operation of the loop for a particular value of ω_n/ω_{step} and for various values of ζ. Figure 9 compares the maximum permissible F_{max}/F_{min} of the C-PFD and of WS-PFDs for loops with $\zeta=0.707$ and ω_n/ω_{step} in the range [1/200, 1/20].

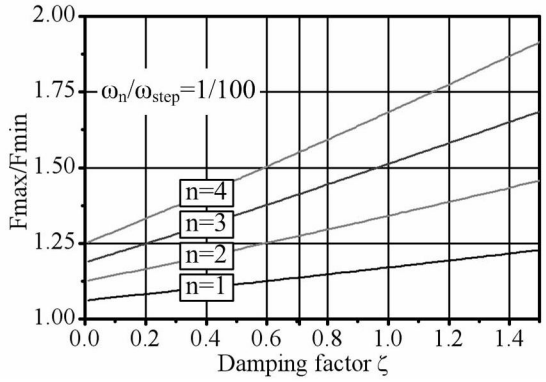

Figure 8. Fmax over Fmin ratio of a synthesizer with various PFDs for cycle slipping free operation.

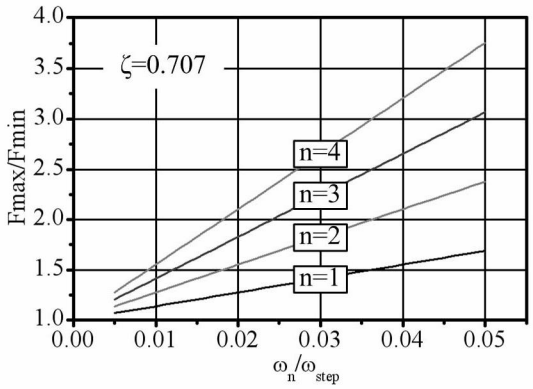

Figure 9. Fmax over Fmin ratio of a synthesizer with various PFDs for cycle slipping free operation.

As a design rule, the ratio ω_n/ω_{step} should not exceed 1/10 [5, 6, 7] to avoid stability issues due to the discrete nature of the PFD. In conventional applications it is selected as 1/100, or even smaller [6, 7]. For loops with $\omega_n/\omega_{step}=1/100$, $\zeta=0.707$ and $n=1$ (C-PFD) the F_{max}/F_{min} ratio should not exceed 1.13781, or else cycle slipping will occur. It is evident that PLLs used in applications where wide bandwidth coverage is required, could benefit significantly by incorporating a WS-PFD.

V. Conclusion

A phase detector with a wide linear operating range, exceeding the ±2π limitation, and a saturation mechanism was presented in this paper. The so called WS-PFD, unlike the conventional PFD, can provide to a PLL all the advantages that linear theory predicts, i.e. cycle slipping free operation and a predefined settling time that does not depend on the frequency step applied to the PLL input. Applications involving wide frequency coverage or multiband operation, could undoubtedly take advantage by incorporating a WS-PFD in the PLL, which can replace C-PFD without the need of redesigning the loop. All the above, in conjunction with the relatively low circuit complexity and the anticipated low power consumption, render WS-PFD a rather competitive phase detector. As future work, the case of a nonlinear transfer characteristic with gradually increasing gain, yet with saturation, could be investigated.

References

[1] V. F. Kroupa, "Phase Lock Loops and Frequency Synthesis," John Wiley & Sons, 2003.

[2] R. E. Best, "Phase-Locked Loops: Theory, Design and Applications, Fifth Edition," McGraw-Hill, 2003.

[3] D. R. Stephens, "Phase-Locked Loops for wireless communications: Digital, Analog and Optical Implementations, Second Edition," Kluwer Academic Publishers, 2002.

[4] K. Kundert, "Predicting the Phase Noise and Jitter of PLL-Based Frequency Synthesizers," www.designers-guide.com.

[5] B. Razavi, "RF Microelectronics," Prentice Hall, 1998.

[6] F. M. Gardner, "Charge-Pump Phase-Locked Loops," IEEE Trans. Comm., Vol. COM-28, pp.1849-1858, November 1980.

[7] D. Banerjee, "PLL Performance, Simulation, and Design, 3rd Edition," 2003.

[8] P. V. Brennan, "Performance of phase-locked loop frequency synthesizer using accumulative phase detector," IEE Proc. – Circuits Devices Syst., Vol. 143, No. 5, pp. 249-254, October 1996.

[9] G. T. Roh, Y. H. Lee, and B. Kim, "Optimum Phase-Acquisition Technique for Charge-Pump PLL," IEEE transactions on Circuits and Systems-II: Analog and Digital Signal Processing, Vol. 44, No. 9, pp. 729-740, September 1997.

[10] C. Y. Yang and S. I. Liu, "Fast-Switching Frequency Synthesizer with a Discriminator-Aided Phase Detector," IEEE Journal of Solid-State Circuits, Vol. 35, NO. 10, pp. 1445-1452, October 2000.

[11] I. C. Hwang, S. H. Song, and S. W. Kim, "A Digitally Controlled Phase-Locked Loop With a Digital Phase-Frequency Detector for Fast Acquisition," IEEE Journal of Solid-State Circuits, Vol. 36, No. 10, pp. 1574-1581, October 2001.

[12] J. Lee, and B. Kim, "A Low-Noise Fast-Lock Phase-Locked Loop with Adaptive Bandwidth Control," IEEE Journal of Solid-State Circuits, Vol. 35, No. 8, pp. 1137-1145, August 2000.